Chapter 4: Design of Amplifiers and Controlled Sources

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1 Introduction

In the last chapter, we studied the realization of current-controlled sources with and without active-feedback. We will begin this chapter by realizing voltage-controlled sources, and further study techniques to linearize them. We will then focus on obtaining transistor-based realizations of linear voltage-controlled sources using linear, bilateral, passive feedback structures.

We will then coonsider techniques for realizing high-gain stages leading to the evolution of the operational amplifier.

2 Transconductor Amplifiers using Active Elements

Consider the MOSFET shown in figure 1. The current, i_0, is related to the terminal voltages by

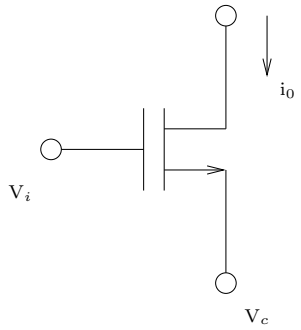

Figure 1: MOS transistor in the Saturation Region

$$i_0 = \frac{k}{2}\left(V_i - V_c - V_T\right)^2 \tag{1}$$

$$g_m = \frac{\partial i_0}{\partial v_i} = k\left(V_i - V_c - V_T\right) \tag{2}$$

$$V_i > V_c + V_T$$

2.1 Quasi-Differential Operation

To obtain a linear transconductor using the MOS transistor shown in figure 1, we can use the quasi-differential structure shown in figure 2

The differential output current, i_{0a} - i_{0b}, can be computed using the following equations.

$$i_{0a} = \frac{k}{2}\left(V_{ia} - V_c - V_T\right)^2 \tag{3}$$

$$i_{0b} = \frac{k}{2}\left(V_{ib} - V_c - V_T\right)^2 \tag{4}$$

$$i_{0a} - i_{0b} = \frac{k}{2}\left(V_{ia} + V_{ib} - 2\left(V_c + V_T\right)\right)\left(V_{ia} - V_{ib}\right) \tag{5}$$

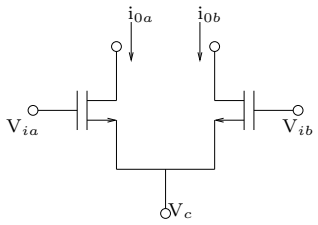

Figure 2: Quasi-Differential Transconductor

Choosing $V_{ia} = V_{c0} + \frac{\Delta v_i}{2}$ and $V_{ib} = V_{c0} - \frac{\Delta v_i}{2}$, equation 5 reduces to

$$i_{0a} - i_{0b} = \frac{k}{2}\left(2V_{c0} - 2\left(V_c + V_T\right)\right)\Delta v_i \tag{6}$$

a linear amplifier as long as the two transistors remain in current-saturation region. The transconductance of the circuit is given by

$$G_m = k\left(V_{c0} - \left(V_c + V_T\right)\right) \tag{7}$$

and can be varied *linearly* by changing V_{c0} or V_c, the common-mode voltages. For simplicity, V_c can be made zero.

Let us now consider a similar architecture with the BJT. The circuit is shown in figure 3

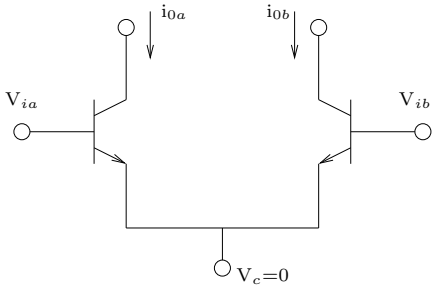

Figure 3: Differential Transconductor using BJTs

The following equations describe the behaviour of this circuit

$$i_{0a} = I_{e0}e^{\frac{V_{ia}}{V_t}} \tag{8}$$

$$i_{0b} = I_{e0}e^{\frac{V_{ib}}{V_t}} \tag{9}$$

$$\frac{i_{0a}}{i_{0b}} = e^{\left(\frac{V_{ia}-V_{ib}}{V_t}\right)} \tag{10}$$

a relation that is independent of the device active parameter!

Using equation 10, and further assuming that the common point between the two emitter is now connected to a current source, I_0, we can also write

$$\frac{i_{0a} - i_{0b}}{i_{0a} + i_{0b}} = \frac{\Delta i_0}{I_0} \tag{11}$$

$$= \frac{1 - e^{\frac{\Delta v_i}{V_t}}}{1 + e^{\frac{\Delta v_i}{V_t}}} \tag{12}$$

$$= tanh\frac{\Delta v_i}{V_t} \tag{13}$$

Equation 13 is the famous tan-hyperbolic relationship between the output current and the input voltage for a BJT-based differential transconductor. A typical response is shown in figure 4. For this example, the tail current is assumed to be 1mA.

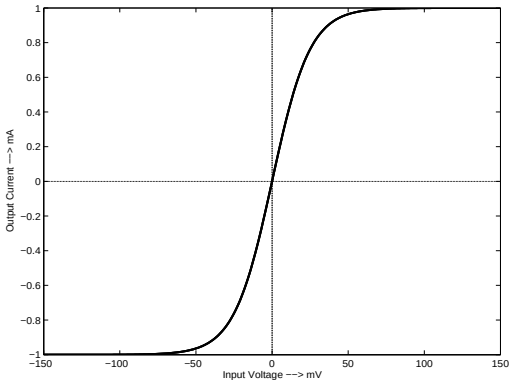

Figure 4: Differential Transconductor I-V Characteristic

Note that for inputs more than $3V_t$ away from the origin, all the current flows through one of the arms. This, hence, indicates the logical evolution of a *Differential Transconductor* using Bipolar Transistors primarily for generating a *Saturating Non-linearity* with *perfectly predictable* characteristic with respect to the differential input signal. This is a very powerful technique to convert differential voltage to differential current output. At this point of time, it is also necessary to mention that all the architectures we have discussed so far (including the translinear networks in chapter 3) for BJTs are also valid for MOSFET structures in the *sub-threshold* region, where just like the BJTs, the drain current exhibits an exponential dependence on the gate-source voltage.

This circuit can also be used for current division or current attenuation. We can express the collector current of any one of the transistors as a function of the total bias current as

$$\frac{i_{0a}}{i_{0a} + i_{0b}} = \frac{i_{0a}}{I_0} \tag{14}$$

$$= \frac{1}{1 + e^{\frac{-\Delta v_i}{V_t}}} \tag{15}$$

$$\frac{i_{0b}}{i_{0a} + i_{0b}} = \frac{1}{1 + e^{\frac{\Delta v_i}{V_t}}} \tag{16}$$

We will later see how this scheme can be used in Automatic Gain Control or Automatic Volume Control structures. The transconductance, g_m, for the circuit is given by

$$g_m = \frac{\partial i_0}{\partial v_i} = \frac{\frac{\partial i_0}{\partial v_e}}{\frac{\partial v_i}{\partial v_e}} \tag{17}$$

$$= \frac{1}{\frac{\partial v_{BEa}}{\partial i_{Ea}} + \frac{\partial v_{BEb}}{\partial i_{Eb}}} \tag{18}$$

$$= \frac{1}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = \frac{1}{\frac{V_t}{i_{Ea}} + \frac{V_t}{i_{Eb}}} \tag{19}$$

$$= \frac{\frac{I_0}{2V_t}}{1 + cosh\frac{\Delta v_i}{V_t}} \tag{20}$$

Figure 5 shows the dependence of the transconductance on the input voltage. The tail current is assumed to be 1mA

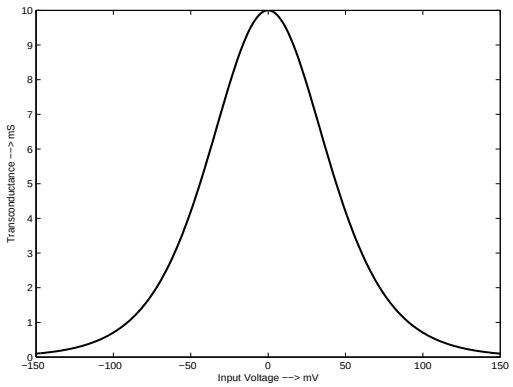

Figure 5: g_m of the Differential Transconductor

It is clear from figure 5 that the linearity of the differential transconductor is rather poor. One method to linearize the transconductance is to add another transconductance in parallel, but with an offset voltage. The offset can be achieved by choosing the transistor sizes appropriately [3].

For the case of two transconductors in parallel, the offset voltage is about $1.375V_t$.

2.2 CMOS Inverter as a Transconductor

If the CMOS inverter could be used as a transconductor, it would be the simplest amplifier architecture ever thought of, and would be highly suitable for VLSI for high-frequency applications. The advantages of such an architecture are the following

1. It does not need any other device other than the active devices
2. It has the minimum number of terminals possible: input, output, supply and ground, and hence, has the lowest number of capacitors to be charged

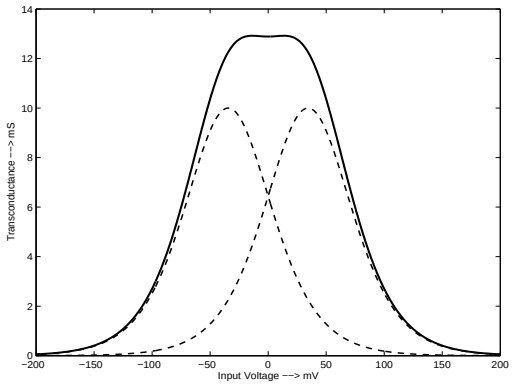

Figure 6: Linearizing the Transconductance by Connecting Transconductors in Parallel

3. It is the only universal building block that can be common to both Analog design and Digital design

Let us begin our discussion by considering the CMOS inverter shown in figure 7.

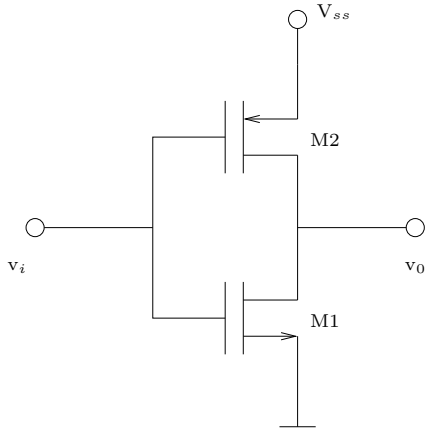

Figure 7: CMOS Inverter

We will restrict our discussion to the region where both the transistors are in current-saturation. If M1 and M2 are in current saturation, we know that

$$\frac{k_p}{2}\left(V_{ss}-V_{iQ}-|V_{Tp}|\right)^2 = \left(V_{iQ}-V_{Tn}\right)^2\frac{k_n}{2} \quad (21)$$

$$V_{iQ}\left(\sqrt{\frac{k_n}{k_p}}+1\right) = V_{Tn}\sqrt{\frac{k_n}{k_p}}+V_{ss}-|V_{Tp}| \quad (22)$$

$$V_{iQ} = \frac{V_{Tn}\sqrt{\frac{k_n}{k_p}}+V_{ss}-|V_{Tp}|}{\sqrt{\frac{k_n}{k_p}}+1} \quad (23)$$

This is the region where $\frac{\Delta v_0}{\Delta v_i}$ is very large. Since we have assumed $\lambda_n = \lambda_p = 0$, the gain is ∞. In this region, the CMOS inverter is useful as an Op-Amp. The input is a nullator for sustaining any output as long as M1 and M2 are in current-saturation. In other words, as long as the output voltage satisfies

$$v_{iQ} - V_{Tn} \le v_0 \le v_i + |V_{Tp}| \quad (24)$$

the CMOS inverter is useful as an op-amp.

If $V_{Tn} = |V_{Tp}|$, and $k_n = k_p$, $V_{iQ} = \frac{V_{ss}}{2}$ and the behaviour is the same as that of an *ideal comparator* using a single power supply. The input is compared with a reference of $\frac{V_{ss}}{2}$. If a dual supply is used, the active region (region where the inverter behaves as an op-amp) occurs at $V_{iQ} = 0$. If the threshold voltages of M1 and M2 are unequal, the active region occurs around an offset voltage given by

$$V_{iQ} = \frac{V_{Tn}\sqrt{\frac{k_n}{k_p}}-|V_{Tp}|}{1+\sqrt{\frac{k_n}{k_p}}} = V_{offset} \quad (25)$$

Let us now assume that λ_n and λ_p take on non-zero values, and see what happens in the active region. The output conductance of the two transistors can be expressed as

$$g_{dsn} = \lambda_n I_{DSQ} \quad (26)$$

$$g_{dsp} = \lambda_p I_{DSQ} \quad (27)$$

The quiescent current can be expressed as

$$I_{DSQ} = \frac{k_n}{2}\left(V_{iQ}-V_{Tn}+V_{ss}\right)^2 \quad (28)$$

$$= \frac{k_n}{2}\left[\frac{V_{Tn}\sqrt{\frac{k_n}{k_p}}-|V_{Tp}|}{1+\sqrt{\frac{k_n}{k_p}}}-V_{Tn}+V_{ss}\right]^2 \quad (29)$$

$$= \frac{k_n}{2}\left[\frac{-|V_{Tp}|+V_{Tn}}{1+\sqrt{\frac{k_n}{k_p}}}+V_{ss}\right] \quad (30)$$

The voltage gain is given by

$$\frac{\Delta v_0}{\Delta v_i} = -\frac{g_{mn} + g_{mp}}{g_{dsn} + g_{dsp}} \tag{31}$$

Assuming $g_{mn} = g_{mp} = g_m$, $g_{dsn} = g_{dsp} = g_{ds}$ and $\lambda_n = \lambda_p = \lambda$, equation 31 reduces to

$$\frac{\Delta v_0}{\Delta v_i} = -\frac{g_m}{g_{ds}} \tag{32}$$

$$= -\frac{\sqrt{2kI_{DSQ}}}{\lambda I_{DSQ}} \tag{33}$$

$$\frac{\Delta v_0}{\Delta v_i} = -\left[\frac{\sqrt{\frac{2k}{I_{DSQ}}}}{\lambda}\right] \tag{34}$$

It would be worthwhile to note here that if the transistors were operating in the sub-threshold region, the gain would be independent of the operating current (since the transconductance is proportional to the current)

We will now see how this structure can be used as a transconductor. Consider the schematic shown in figure 8

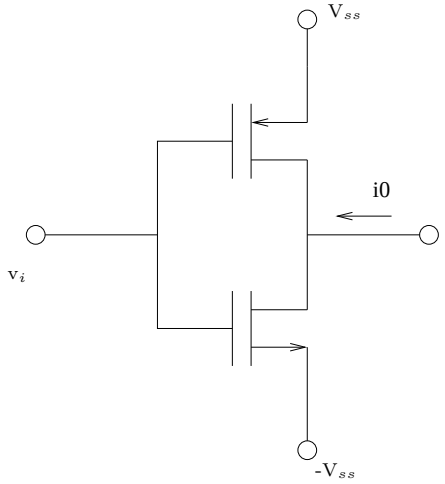

Figure 8: CMOS Inverter as a Transconductor

If the two transistors are in saturation, and assuming that $k_n = k_p = k$ and $V_{Tn} = |V_{Tp}| = V_T$, we can write

$$i_0 = \frac{k}{2}(V_i + V_{ss} - V_T)^2 - \frac{k}{2}(V_{ss} - V_T - V_i)^2 \tag{35}$$

$$= 2k(V_{ss} - V_T)V_i \tag{36}$$

$$= G_m V_i \tag{37}$$

where $G_m = 2k(V_{ss} - V_T)$.

The transconductance can be linearly varied by varying V_{ss}. Since this is a voltage-controlled transconductor, it can act as a modulator or a mixer. If we have

$$V_{ss} = V_{sq} + V_p sin(\omega_m t) \quad \text{modulating frequency} \tag{38}$$

$$V_i = V_p^{'} sin(\omega_c t) \quad \text{carrier frequency} \tag{39}$$

the output current, i_0, is given by

$$i_0 = 2k(V_{sq} + V_p sin(\omega_m t) - V_T) V_p^{'} sim(\omega_c t) \tag{40}$$

$$= 2k(V_{sq} - V_T) V_p^{'} sin(\omega_c t) + 2kV_p V_p^{'} sin(\omega_m t) sin(\omega_c t) \tag{41}$$

an amplitude modulated waveform.

In deriving equation 37, we had assumed that $k_n = k_p$ and $V_{Tn} = |V_{Tp}|$. Both of these conditions are almost impossible to achieve across process variations. One possible solution is to use a composite MOS structure (an NMOS in series with a PMOS) as shown in figure 9 [2].

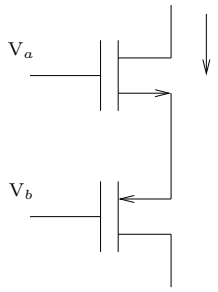

Figure 9: Composite MOS Structure

The difference between the gate voltages can be expressed as

$$V_a - V_b = V_{GSn} + |V_{GSp}| \tag{42}$$

$$= V_{Tn} + \sqrt{\frac{2I_{DS}}{k_n}} + |V_{Tp}| + \sqrt{\frac{2I_{DS}}{k_p}} \tag{43}$$

$$= V_T + \sqrt{\frac{2I_{DS}}{k}} \tag{44}$$

where,

$$V_T = V_{Tn} + |V_{Tp}| \tag{45}$$

$$\frac{1}{\sqrt{k}} = \frac{1}{\sqrt{k_n}} + \frac{1}{\sqrt{k_p}} \tag{46}$$

This structure can now be used as a current source or a current sink. The inverter can now be modified as shown in figure 10 to obtain a linear transconductor.

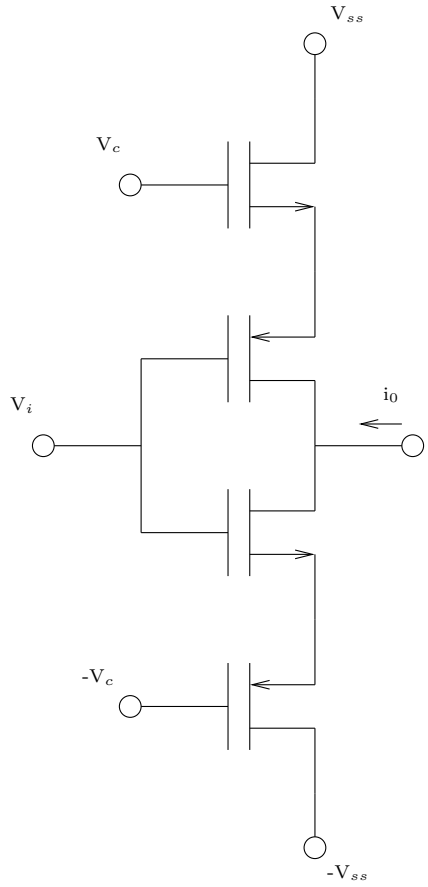

Figure 10: Modified CMOS Inverter

The output current, i_0, is given by

$$\begin{aligned} i_0 &= 2kV_i\left(V_c - V_T\right) && (47)\\ &= 2k\left(V_c - V_T\right)V_i && (48)\\ &= G_m V_i && (49) \end{aligned}$$

Since we have cascaded devices vertically in this structure, it will require higher supplies than a single CMOS inverter. An alternate approach is to use two CMOS inverters in quasi-differential mode as shown in figure 11. A demonstration of a G_m-C filter based on this technique to cancel the second-order term, and gain-enhancement using negative-resistance synthesis can be found in [1].

The output currents, i_{01} and i_{02}, are given by

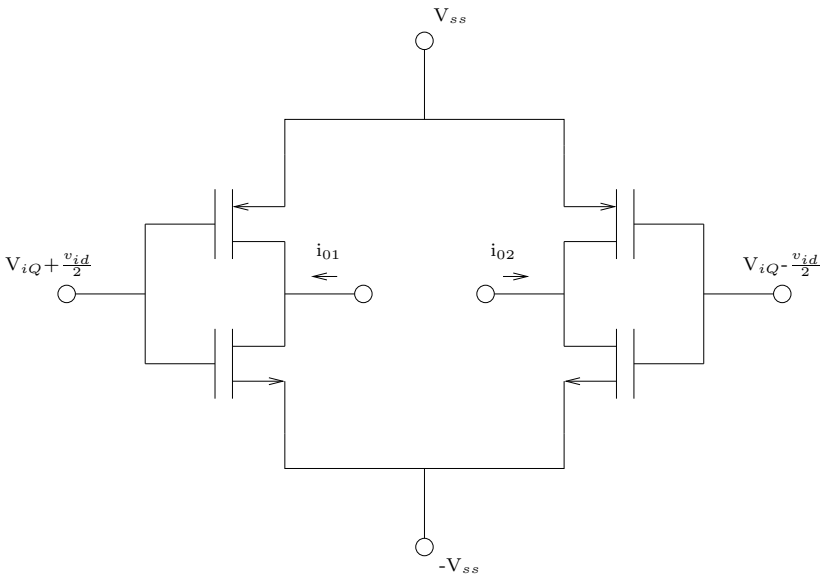

Figure 11: Quasi-Differential CMOS Inverter

$$i_{01} = \frac{k_n}{2}\left(V_{iQ} + \frac{v_{id}}{2} - V_{Tn} + V_{ss}\right)^2 - \frac{k_p}{2}\left(V_{ss} - V_{iQ} - \frac{v_{id}}{2} - |V_{Tp}|\right)^2 \quad (50)$$

$$i_{02} = \frac{k_n}{2}\left(V_{iQ} - \frac{v_{id}}{2} - V_{Tn} + V_{ss}\right)^2 - \frac{k_p}{2}\left(V_{ss} - V_{iQ} + \frac{v_{id}}{2} - |V_{Tp}|\right)^2 \quad (51)$$

The differential output current, i_0, is given by

$$i_0 = i_{01} - i_{02} \quad (52)$$

$$= k_n\left(V_{iQ} + V_{ss} - V_{Tn}\right)v_{id} + k_p\left(V_{iQ} + V_{ss} - |V_{Tp}|\right)v_{id} \quad (53)$$

$$= \left[\left(k_n + k_p\right)\left(V_{ss} + V_{iQ}\right) - \left(k_n V_{Tn} + k_p\left|V_{Tp}\right|\right)\right]v_{id} \quad (54)$$

3 Feedback Amplifiers using Passive Feedback Structures

In this section, we will consider linearization techniques that use passive elements as feedback structures. We will also describe one technique that can be used to obtain the various properties of a composite feedback structure such as input impedance, output impedance, forward-transmission parameter, and loop-gain. We will begin our discussion with the transconductance amplifier.

3.1 Transconductance Amplifier

Let us say that we would like to realize an ideal transconductor; in other words, an ideal voltage-controlled current-source (VCCS). An ideal VCCS will have infinite input and output resistance and can only be described by the

Y-matrix (shown in equation 55). In order to achieve this, the feedback must appear in series at both terminals.

$$Y_{ideal} = \begin{bmatrix} 0 & 0 \\ \frac{1}{R_s} & 0 \end{bmatrix} \tag{55}$$

The circuit is shown in figure 12. To ease the computation of the loop gain, we need to choose the type of 2-port parameter that we will work with. In this case, the feedforward and feedback structures come in series, and hence, the input and output currents will be the same. So, if we were to express the feedforward and feedback blocks in terms of their Z parameters, the composite Z-parameter will simply be the sum of the individual Z-parameters. The response of the system can then be obtained by inverting the composite Z-matrix (the result will be a Y-matrix that characterizes the transconductor). We will refer to such a feedback as Z-feedback.

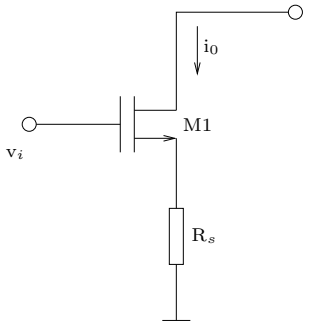

Figure 12: Transconductor Amplifier using Series Feedback

Let us now calculate the input impedance, output impedance, transconductance and loop-gain of this feedback structure. To do so, we will begin with the Z-parameters of the amplifier and the feedback structure.

The Z-parameters of the feedback network and the amplifier are given respectively by

$$Z_r = \begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix} \tag{56}$$

$$Z_f = \begin{bmatrix} R_i & 0 \\ -R_i g_m r_{ds} & r_{ds} \end{bmatrix} \tag{57}$$

where R_i is the input impedance, g_m is the transconductance and r_{ds} is the output resistance of the transistor.

The composite Z-matrix is given by

$$Z_{comp} = \begin{bmatrix} R_i + R_s & R_s \\ -R_i g_m r_{ds} + R_s & R_s + r_{ds} \end{bmatrix} \tag{58}$$

The loop-gain of this structure is given by

$$g_l = \frac{-R_i g_m r_{ds} R_s}{(R_i + R_s)(R_s + r_{ds})} \tag{59}$$

The composite Y-matrix (Remember that an ideal transconductor - VCCS - can only be characterized by the Y-matrix) is obtained by inverting the composite Z-matrix of equation 58 and is given by

$$Y_{comp} = \begin{bmatrix} \frac{R_s+r_{ds}}{\Delta Z} & \frac{-R_s}{\Delta Z} \\ \frac{-R_i g_m r_{ds}}{\Delta Z} & \frac{R_i+r_{ds}}{\Delta Z} \end{bmatrix} \tag{60}$$

where,

$$\Delta Z = (R_i + R_s)(R_s + r_{ds}) + R_i g_m r_{ds} R_s \tag{61}$$

Further simplification of equation 60 yields,

$$Y_i = \frac{1}{(R_i + R_s)(1 - g_l)} \tag{62}$$

$$Y_0 = \frac{1}{(R_s + R_{ds})(1 - g_l)} \tag{63}$$

$$Y_f = \frac{1}{R_s + \frac{(R_i+R_s)(R_s+r_{ds})}{R_i g_m r_{ds}}} \tag{64}$$

It is clear from equations 62 and 63 that the input and output impedances are scaled by a factor $1 - g_l$. This is a property of feedback as we saw in chapter 2. It must also be noted that we can arrive at the well-known expression for Y_f ($Y_f = R_s + \frac{1}{g_m}$) by using $R_i \gg R_s$ and $r_{ds} \gg R_s$ in equation 64.

3.2 Transresistor Amplifier

The transresistor amplifier (figure 13) is the dual of the transconductance amplifier that we discussed in the earlier section. Here, the feedback appears in shunt at both the input and the output (the feedback appears in shunt because an ideal transconductance amplifier has zero input and output impedance), and the feedforward and feedback blocks have the same input and output voltages. Hence, we will use the Y-parameters for computing the properties of the composite structure. This type of feedback is called Y-feedback.

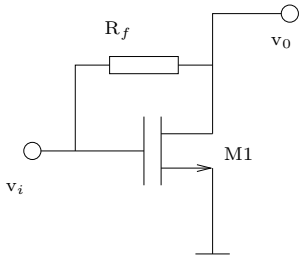

Figure 13: Transresistor Amplifier using Shunt Feedback

Proceeding along the same lines as we did for the transconductance amplifier, we will begin by writing the Y-matrix for the amplifier and the feedback network.

$$Y_r = \begin{bmatrix} \frac{1}{R_f} & -\frac{1}{R_f} \\ -\frac{1}{R_f} & \frac{1}{R_f} \end{bmatrix} \tag{65}$$

$$Y_f = \begin{bmatrix} 0 & 0 \\ g_m & g_{ds} \end{bmatrix} \tag{66}$$

Note that since the independent variable at the input is voltage, we need not assume any input resistance for the transistor (We would not have been able to calculate the Z parameters if we had not assumed a finite input resistance) in this case. The composite Y-parameters are given by

$$Y_{comp} = \begin{bmatrix} \frac{1}{R_f} & -\frac{1}{R_f} \\ g_m - \frac{1}{R_f} & \frac{1}{R_f} + g_{ds} \end{bmatrix} \tag{67}$$

The loop gain, g_l, is given by

$$g_l = -\frac{g_m - \frac{1}{R_f}}{\frac{1}{R_f} + g_{ds}} \tag{68}$$

The input and output resistances will hence be given by

$$Z_i = \frac{1}{\left(\frac{1}{R_f}\right)(1 - g_l)} \tag{69}$$

$$Z_0 = \frac{1}{\left(g_{ds} + \frac{1}{R_f}\right)(1 - g_l)} \tag{70}$$

and the forward transmission parameter, Z_f, is given by

$$Z_f = -\frac{\left(g_m - \frac{1}{R_f}\right) R_f}{g_{ds} + g_m} \tag{71}$$

and simplifies to Z_f = - R_f, if $g_m \gg \frac{1}{R_f}, g_m \gg g_{ds}$.

3.3 Voltage-Controlled Voltage Sources and Current-Controlled Current-Sources

To better understand the realization of these controlled-sources, let us begin by considering the nullator-norator equivalent of the VCVS shown in figure 14.

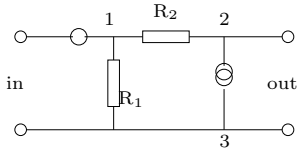

Figure 14: Nullator-Norator Equivalent of a VCVS

It is clear from the figure that a VCVS cannot be realized as a single-transistor structure since the nullator and norator do not share a junction. Since the CCCS is simply the dual of this circuit, the result holds there as well.

Hence, the lowest number of transistors required to realize a VCVS or a CCCS is two. There are two possible methods of realizing such circuits. One option is to cascade a VCCS(CCVS) with a CCVS(VCCS) to get a VCVS(CCCS). The other option is to connect an open-circuit (norator and nullator in series) either between nodes 1 and 2 or between nodes 1 and 3 in the figure. By proper pairing of nullators and norators, one can then realize two-transistor loop based VCVS or CCCS. We will now consider both these techniques.

Figure 15 shows the single-ended realization of a VCVS obtained by cascading a VCCS with a CCVS. In such a circuit, the input impedance is determined by the first stage (VCCS) and the output impedance is determined by the second stage (CCVS). The voltage gain is given by $\frac{R_f}{R_s}$.

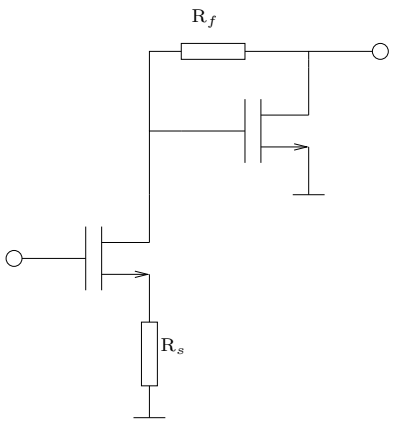

Figure 15: VCVS Obtained as a Cascade of VCCS and CCVS

A fully balanced version of this circuit can be obtained by

1. Drawing the Mirror-Image of the Circuit
2. Biasing N-channel MOSFETS in the Active Region by connecting drains of all MOSFETs to VDD through resistors
3. Lifting the common-source points of the symmetric structuerthrough bias current-sources to negative supply

The resulting circuit is shown in figure 16. Such a circuit can be used as fully-biased differential video amplifier IC or a wide-band IC.

The alternate approach is to use two-transistor loops with overall feedback. Since we have cascaded two stages, this structure exhibits higher dc gain. Needless to say, we also have to contend with multiple poles within the loop, and frequency compensation will in all likelihood be required to stabilize the structure (We looked at system-level frequency compensation in chapter 2. We will look at circuit-level techniques later in this chapter when we discuss the design of operational amplifiers). Figures 17 and 18 show the VCVS and CCCS realizations, respectively while equations 72 and 73 show the ideal g and h-matrix, respectively.

$$G = \begin{bmatrix} 0 & 0 \\ 1 + \frac{R_2}{R_1} & 0 \end{bmatrix} \tag{72}$$

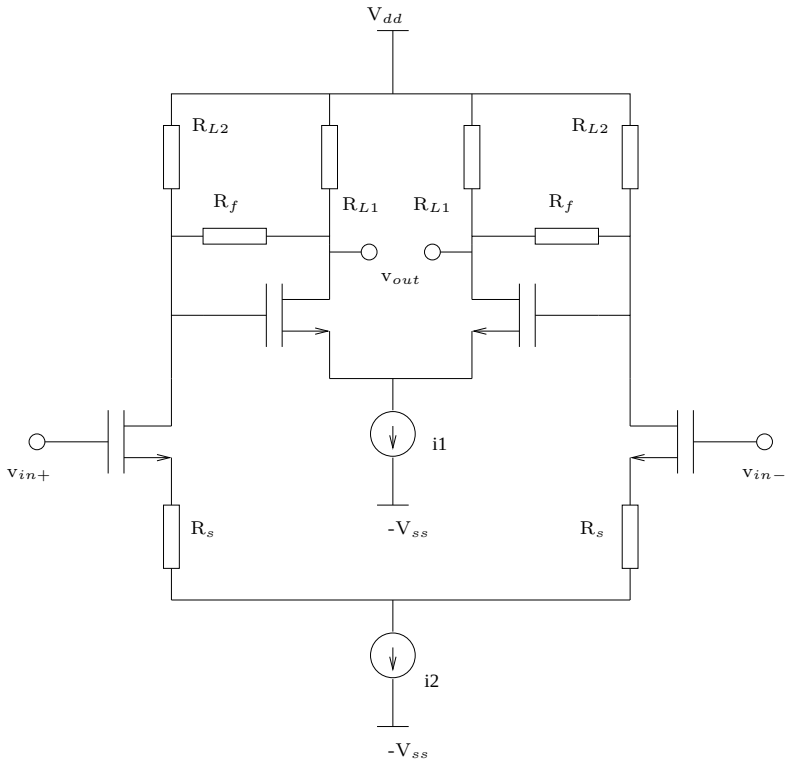

Figure 16: Differential Realization of a VCVS

$$H = \begin{bmatrix} 0 & 0 \\ -\left(1+\frac{R_2}{R_1}\right) & 0 \end{bmatrix} \tag{73}$$

The reader is strongly urged to verify that the VCVS(CCCS) is indeed a h-feedback(g-feedback) structure, compute the composite matrix, and prove that the feedback increases(decreases) the input impedance and decreases(increases) the output impedance. We will now consider composite feedback structures. In other words, structures that use more than one kind of feedback arrangement.

3.4 Composite Feedback Structures

Consider the schematic shown in figure 19.

If the active device (in this case, the combination of M1 and R$_e$) were a nullor, the gain of such an amplifier will be given by

$$g = \frac{v_0}{v_s} = -\frac{R_f}{R_s} \tag{74}$$

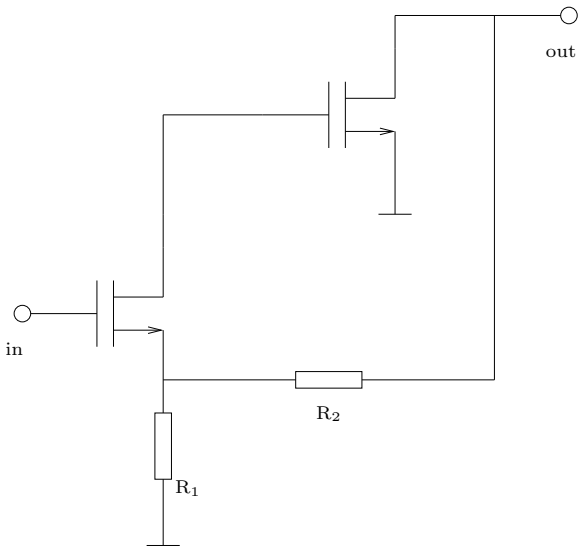

Figure 17: VCVS Realization using two-transistor H-feedback Structure

In this case, though, the presence of R_e results in finite active-device gain, thereby modifying the gain of the amplifier. The intermediate voltage gain, $\frac{v_0}{v_i}$, can be calculated using

$$\frac{v_i}{R_e + \frac{1}{g_m}} = \frac{v_i - v_0}{R_f} - \frac{v_0}{R_L} \tag{75}$$

$$v_i \left(\frac{1}{R_e + \frac{1}{g_m}} - \frac{1}{R_f} \right) = -v_0 \left(\frac{1}{R_f} + \frac{1}{R_L} \right) \tag{76}$$

$$\frac{v_0}{v_i} = -\frac{\frac{1}{R_e + \frac{1}{g_m}} - \frac{1}{R_f}}{\frac{1}{R_f} + \frac{1}{R_L}} \tag{77}$$

$$\approx -\frac{R_f \parallel R_L}{R_e} \tag{78}$$

The input impedance, R_i, is given by

$$\frac{v_i}{R_i} = \frac{v_i - v_0}{R_f} \tag{79}$$

$$R_i = \frac{1 + \frac{R_f \| R_L}{R_e}}{R_f} \tag{80}$$

Note that the input impedance is determined by the element that appears in shunt at the input (in this case, the feedback resistance, R_f).

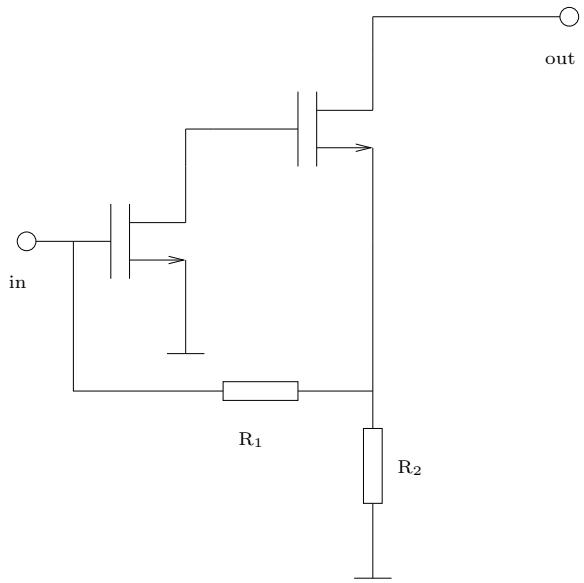

Figure 18: CCCS Realization using two-transistor G-feedback Structure

The overall voltage gain, $\frac{v_0}{v_s}$, can now be simplified as

$$\frac{v_0}{v_s} = \frac{v_0}{v_i} \cdot \frac{v_i}{v_s} \tag{81}$$

$$= -\frac{R_f \parallel R_L}{R_e} \cdot \frac{R_i}{R_i + R_s} \tag{82}$$

The output resistance is calculated by computing the driving point impedance at the output with the input source shorted to ground. In such a case, v_i, the voltage at the gate of the M1 reduces to

$$v_i = \frac{R_s}{R_s + R_f} \cdot v_0 \tag{83}$$

Assuming that the transistor is a nullor, the same voltage is seen at the source terminal of the transistor as well. Hence, the current through R_e is given by

$$i_s = \frac{R_s}{R_s + R_f} \cdot \frac{v_0}{R_e} \tag{84}$$

The output current, i_0, is the sum of the currents flowing through R_f and R_e and is given by

$$i_0 = v_0 \left(\frac{R_s}{R_f + R_s} \cdot \frac{1}{R_e} + \frac{1}{R_f + R_s} \right) \tag{85}$$

The output resistance then simplifies to

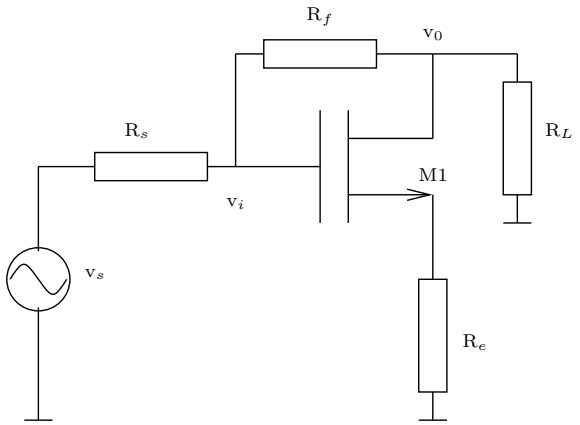

Figure 19: Amplifier using Composite Feedback: Y and Z

$$R_0 = \frac{v_0}{i_0} = \frac{1}{\left(\frac{R_s}{R_f+R_s} \cdot \frac{1}{R_e} + \frac{1}{R_f+R_s}\right)} \tag{86}$$

Such a circuit has well-defined input and output impedances and can be used in circuits that require impedance matching. One can also realize two-transistor h-g composite-feedback based structures. These structures exhibit higher loop gain, and also have more degrees of freedom than the single-transistor amplifier. We will present a very simplified analysis of such a structure here. The reader is referred to [4] for a practical implementation.

Consider the circuit shown in figure 20. (It must be noted that what is shown in the figure is the AC signal-picture - The DC voltage supply is hence shorted out and the load resistors are connected to ground)

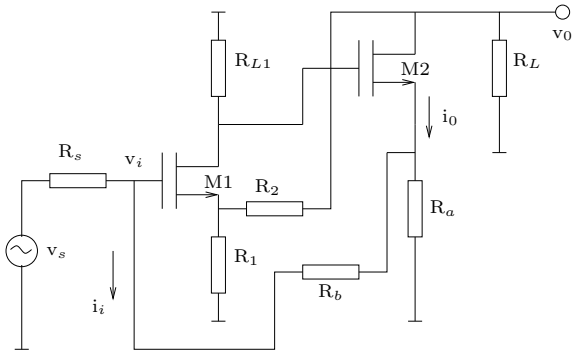

Figure 20: Amplifier using Composite Feedback: H and G

The voltage gain is determined by h-feedback (shunt) and the current gain is determined by g-feedback (series). The intermediate voltage and current gains are given by

$$\frac{v_0}{v_i} = 1 + \frac{R_2}{R_1} \tag{87}$$

$$\frac{i_0}{i_i} = -\left(1 + \frac{R_b}{R_a}\right) \tag{88}$$

The input impedance is determined by the shunt element at the input (R_b) while the output impedance is determined by the shunt element at the output (R_2). Let us now compute the input impedance assuming that the output is shorted (to ease calculation). The voltage at the output of the first stage is given by (assuming that M1 is a nullor)

$$v_1 = -\frac{R_{L1}}{R_1 \parallel R_2} \cdot v_i \tag{89}$$

Further assuming that M2 is also a nullor, this voltage will also appear at the source of M2. The current, i_i, through R_b is then given by

$$i_i = \frac{1 + \frac{R_{L1}}{R_1 \parallel R_2}}{R_b} \cdot v_i \tag{90}$$

and the input impedance is given by

$$R_{in} = \frac{v_i}{i_i} = \frac{R_b}{1 + \frac{R_{L1}}{R_1 \parallel R_2}} \tag{91}$$

To calculate the output impedance, we will short the input source and calculate the driving point impedance at the output. For a voltage of v_0 at the output terminal, the current through R_2 is given by (assuming that M1 is a nullor with infinite g_m)

$$i_{R2} = \frac{v_0}{R_2} \tag{92}$$

This current will flow through M1 and generate a drain voltage given by

$$vd_{M1} = \frac{R_{L1}}{R_2} \cdot v_0 \tag{93}$$

Since M2 is a nullor, the same voltage will appear at the source terminal of M2 and generate a current through R_a given by

$$id_{M1} = \frac{R_{L1}}{R_2 \cdot R_a} \cdot v_0 \tag{94}$$

The total current due to v_0 is given by

$$i_0 = \left(\frac{1}{R_2} + \frac{R_{L1}}{R_2 \cdot R_a}\right) \cdot v_0 \tag{95}$$

The output impedance reduces to

$$R_0 = \frac{R_2}{1 + \frac{R_{L1}}{R_a}} \tag{96}$$

What we have provided are very approximate (but nevertheless useful and insightful) expressions for the various parameters of interest. Even with such an approach, we are able to appreciate the roles that various resistances play in determining the behaviour of this circuit.

Other modifications of composite feedback (a cascade of Z and Y to obtain a VCVS and overall G feedback to obtain the CCCS) are possible and have been explored in the literature [5]. These circuits are beginning to find use in the area of wide-band microwave amplifer design.

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