Chapter 3: Basic Building Blocks for Amplifier Design : Active-Device Realization of Controlled and Independent Sources

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1 Transistors as Active Elements

Let us suppose that we have a device which behaves as a transconductor with a transconductance, g_m, given by

$$g_m|_{(I_{0q},V_{iq})} = \frac{\partial i_0}{\partial v_i} \tag{1}$$

where I_{oq} is the quiescent operating current and V_{iq} is the quiescent operating input voltage at which the device remains active (i.e. capable of giving power gain).

We can think of two such devices
(a) one with g_m proportional to I_{0q}
(b) another with g_m proportional to V_{iq}

Let us now consider each of these cases in more detail

$$\begin{aligned}
\frac{\partial i_0}{\partial v_i} &= k \cdot i_0 && (2)\\
\frac{\partial i_0}{i_0} &= k \cdot \partial v_i && (3)\\
\ln i_0 &= k \cdot v_i + c && (4)\\
i_0 &= I_{c0} e^{k v_i} && (5)
\end{aligned}$$

The above equations describe the Bipolar Junction Transistor (BJT). The other type of active device can be realized as shown below.

$$\begin{aligned}
\frac{\partial i_0}{\partial v_i} &= k \cdot v_i + c && (6)\\
i_0 &= \frac{k \cdot v_i^2}{2} + c \cdot v_i + c_1 && (7)\\
&= k_1 \cdot (v_i - V_T)^2 && (8)
\end{aligned}$$

The above equations describe the behaviour of the Metal-Oxide-Semiconductor Field-Effect-Transistor(MOSFET) and the Junction Field-Effect-Transistor(JFET)

These devices perform data expansion (by nature of the exponential/squared relationship between current and voltage) and hence, they can be used in signal processing as data expanders.

Let us now consider these devices in more detail by considering their action in the active region. We will not delve into great detail on either device, but instead understand the basic principle of operation in, and derive a simple equivalent-circuit model for each device. Such a model will suffice for our purposes of understanding the fundamental principles behind the various claases of circuits is vogue today.

1.1 Transistor Action in the Active Region - BJT

A BJT is formed by connecting two p-n junction back to back. To obtain transistor action, one juction is forward-biased while the other is reverse-biased. In very simple terms, the forward-biased (base-emitter) junction *emits* carriers that are *collected* by the reverse-biased (base-collector) junction. The various terminals in a BJT are called *emitter*, *collector* and *base*.

Since there are two types of carriers (electrons and holes), we can visualise two different BJT configurations, namely, the npn configuration and the pnp configuration. Figure 1 shows the symbols, and the current and voltage polarities for both configurations.

In an npn transistor, the emitter *emits* electrons which are *collected* by the collector. When these electrons pass through the base, some of them recombine with the holes in the base. The applied voltage on the emitter-base junction forces additional electrons to be *emitted* from the emitter. To maintain charge neutrality, the base will also source an equal number of holes. This contributes to the base current. The current gain of the BJT is given by the ratio of collector to base current. The current gain of an ideal BJT is infinity.

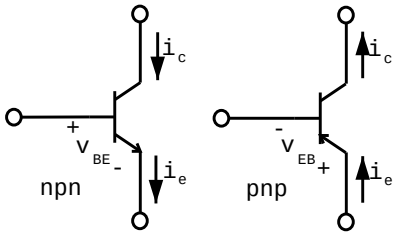

Figure 1: n-p-n and p-n-p Bipolar Junction Transistors (BJTs)

Let us now consider the various equations that describe the behaviour of BJTs.

$$
\begin{aligned}
i_e &= I_{e0} e^{V_{BE}/V_t} && (9)\\
i_c &= \alpha i_e && (10)\\
\text{where } V_t &= \frac{kT}{q} && (11)\\
&= 25 \text{ mV at room temp} && (12)
\end{aligned}
$$

The transconductance of the BJT is given by,

$$
\begin{aligned}
g_m &= \frac{\partial i_c}{\partial v_{BE}} && (13)\\
&= \frac{I_c}{V_t} && (14)\\
&= \frac{qI_c}{kT} && (15)
\end{aligned}
$$

The ideal BJT is shown in figure 2. The g_m is ∞ while Δv_{BE} tends to zero. The base current is zero and the current gain, β, is ∞.

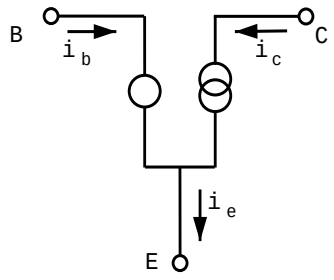

Figure 2: Nullator-Norator Equivalent Circuit of a BJT

To understand the practical effects of BJT-based circuits, a more detailed model is necessary. To realize the detailed model, let us first compute the output resistance. The output resistance in a BJT arises because of base-width modulation. An increasing reverse-bias on the base-collector junction increases the depletion-width of the junction. Depending on the ratio of base to collector doping, the depletion region will extend into the base. This alters the collector current. The effect is described in the following equations.

$$i_c = \alpha I_{s0} e^{V_{BE}/V_t}(1 + \frac{V_{CE}}{V_E}) \quad (16)$$

$$= I_c(1 + \frac{V_{CE}}{V_E}) \quad (17)$$

where V_E is called the Early Voltage. The output resistance is now given by

$$g_{ce} = \frac{\partial i_c}{\partial v_{ce}} \quad (18)$$

$$= \frac{I_{cq}}{V_E} \quad (19)$$

$$r_{ce} = \frac{V_E}{I_{cq}} \quad (20)$$

Depending on the doping of the emitter layer and the dimensions of the emitter 'finger', a parasitic series resistance is present between the intrinsic and extrinsic emitter. The effect of recombination current can be modeled using a resistance between the base and emitter.

$$I_e = g_m V_{BE} \quad (21)$$

$$I_b = \frac{I_e}{\beta + 1} \quad (22)$$

$$= \frac{g_m V_{BE}}{\beta + 1} \quad (23)$$

$$= \frac{V_{BE}}{r_e(\beta + 1)} \quad (24)$$

$$r_{be} = \frac{V_{BE}}{I_b} = r_e(\beta + 1) \quad (25)$$

To obtain a reliable high-frequency model, we should also consider the various capacitances. In addition to the depletion capacitances associated with each junction, there are also a number of parasitic capacitances that need to be considered. The overlap between the base and collector semiconductor layers results in a parasitic base-collector capacitance. A parasitic

capacitance from the collector to ground is also present (and is typically very small in magnitude). In addition, a diffussion capacitance is present between the base and emitter terminals, and is equal to $g_m\tau_f$, where g_m is the transconductance, and τ_f is the transit time. The complete equivalent circuit is shown in figure 3

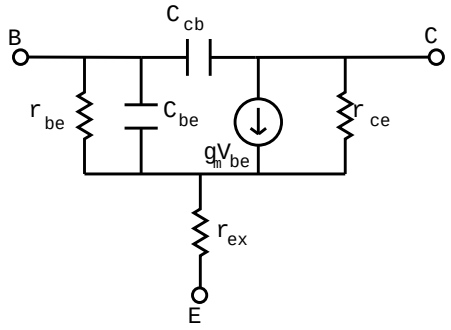

Figure 3: High-Frequency Model of a BJT

1.2 Transistor Action in the Active Region - MOSFET

In a MOS structure, a channel is formed between the source and the drain by applying a voltage on the gate. The drain current saturates in the channel as the drain to source voltage causes the channel to get pinched-off at the drain end. The following equations describe the behaviour of the MOSFET. In the following equations, V_T is the threshold voltage and $K = K_0\frac{W}{L}$

The two kinds of MOS transistors are shown in figure 4.

$$i_{DS} = \frac{k(V_{GS}-V_T)^2}{2}; V_{DS} \geq V_{GS}-V_T \quad (26)$$

$$i_{DS} = k\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]; V_{DS} < V_{GS}-V_T \quad (27)$$

The constant, k, in the above equations is related to the mobility of the carrier, the capacitance of the oxide layer, and the physical dimensions of the device and is given by

$$k = \mu C_{ox}\frac{W}{L} \quad (28)$$

Equation 26 describes the behaviour of a MOSFET in *saturation* region while equation 27 describes the behaviour of a MOSFET in *linear* region.

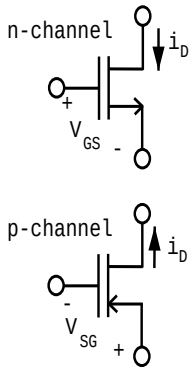

Figure 4: n-channel and p-channel MOS Transistors

Let us now consider the various equations that describe the behaviour of a MOS transistor in the saturation region.

$$g_m = k(V_{GS} - V_T)^2 \tag{29}$$

$$= \sqrt{\frac{2i_D}{k}}k \tag{30}$$

$$= \sqrt{2i_D k} \tag{31}$$

The transconductance can also be represented in terms of the drain current, and the gate-source voltage in the following manner.

$$g_m = \frac{2i_D}{V_{GS} - V_T} \tag{32}$$

The ideal MOS is shown in figure 5. The g_m is ∞ while Δv_{GS} tends to zero. The gate current is zero.

In the pinch-off region, the drain current shows a weak dependence on the drain-source voltage. This effect is known as *channel length modulation* and can be mathematically represented in the following manner.

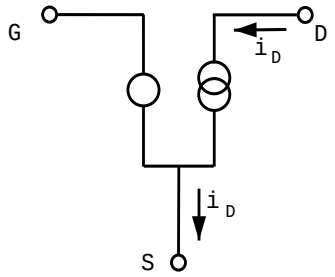

Figure 5: Nullator-Norator Equivalent Circuit of a MOS

$$i_D = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{33}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \approx I_{DSQ}\lambda \tag{34}$$

Let us now consider the various capacitances. The gate-source capacitance is the sum of the oxide capacitance and the overlap capacitance between the gate and the source while the gate-drain capacitance is given by just the overlap capacitance in the saturation region. The equivalent circuit is shown in figure 6. The reader should note that a number of effects have been ignored in the realization of this model. For example, effects like the body effect, the short-channel approximation have not been considered at all. The reader is encouraged to refer other textbooks for a more detailed treatment on the subject [1],[2].

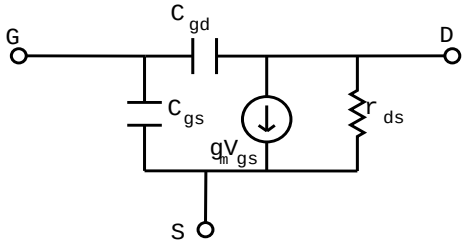

Figure 6: Basic High-Frequency Model of a MOS

2 The Current Mirror

2.1 The Diode-Connected MOSFET

Consider the diode-connected MOSFET shown in figure 7. To analyze this circuit, let us first consider its nullator-norator equivalent. Starting from the nullator-norator equivalent of a MOS transistor shown in figure 5, we can obtain the equivalent of the diode-connected MOSFET by simply shorting the gate and the drain terminals (shown in figure 8).

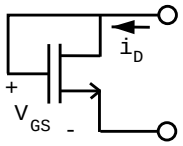

Figure 7: Diode-Connected MOSFET

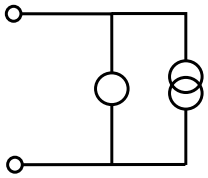

Figure 8: Nullator-Norator Equivalent of a Diode-Connected MOSFET

The equivalent circuit realized for the diode-connected MOSFET is the same as the nullator-norator equivalent for a *Short Circuit*. Hence, this structure can sink any amount of current. In practice, it develops the voltage to sustain any current through it automatically. Here, drain current is the independent variable, and gate-source voltage is the dependent variable.

We can also analyze this as a feedback circuit. The output current is fed back to the input. Further, since the current gain is infinity, the loop gain is infinity. As a result, this circuit will perform the inverse function. In other words, in the forward direction, the relation between input voltage (V_{GS}), and output current (I_D) is a squaring function. Now, due to the large feedback gain, the drain current will generate a gate-source voltage that exhibits a square-root dependence on the current.

This is explained in the following equations.

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \tag{35}$$

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{k}} \tag{36}$$

The same circuit can also be realized by using a BJT instead of a MOS transistor. The input voltage (V_{BE}) would then have a logarithmic relation to the current.

Let us now look at what happens when we use a more detailed equivalent circuit for the MOS transistor. The MOS transistor has a finite g_m and a finite g_{ds}. The resulting circuit is shown in figure 9.

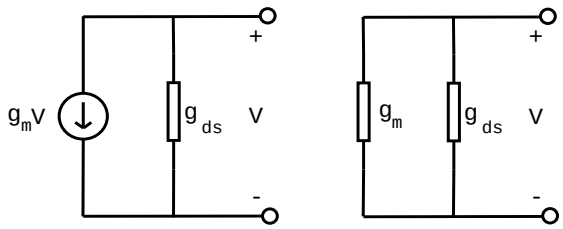

Figure 9: Equivalent Circuit of the Diode-Connected MOSFET

We can now treat this as a *master* transistor to develop the voltage necessary to sustain any current i_D across other *slave* transistors. Letus consider the circuit shown in figure 10

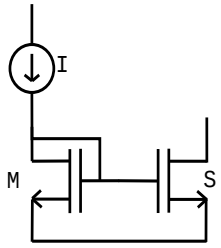

Figure 10: The Current Mirror

The equations that govern the behaviour of the two transistors, M (master) and S (slave) are given below

$$V_{GSM} = \sqrt{\frac{2i_{DM}}{k_M}} + V_{TM} \tag{37}$$

$$V_{GSS} = V_{GSM} \tag{38}$$

$$\sqrt{\frac{2i_{DM}}{k_M}} + V_{TM} = \sqrt{\frac{2i_{DS}}{k_S}} + V_{TS} \tag{39}$$

If the MOSFETs are identical, then we have

$$V_{TS} = V_{TM}; k_M = k_S$$

Then,

$$i_{DS} = i_{DM} = I \tag{40}$$

This is the basis of what is popularly known as the *current mirror*. The *slave* MOSFETs simply reflect the current of the master as long as they are also biased under similar operating conditions. If the two transistors are in saturation, the dependence of the drain current on the drain-source voltage is weak (modeled by the parameter λ). Hence, a different V_{DS} in the *slave* transistor will result in a current difference that is proportional to λ between the slave and the master.

$$\frac{i_{DM}}{i_{DS}} = \frac{k_M(1+\lambda V_{DSM})}{k_S(1+\lambda V_{DSS})} \approx \frac{k_M}{k_S}\left[1+\lambda\left(V_{DSM}-V_{DSS}\right)\right] \tag{41}$$

In the following section, we will try to better understand the current mirror and try to characterise the effect of various mismatches between the master and the slave.

2.2 Effect of Mismatches on Current Scaling

Let us consider the MOSFET current mirror shown in figure 11 (The reader should note that any number of slaves can be connected to the master).

We have,

$$V_{GSM} = V_{GSS} \tag{42}$$

$$\sqrt{\frac{2I_i}{k_M}} + V_{TM} = \sqrt{\frac{2I_0}{k_S}} + V_{TS} \tag{43}$$

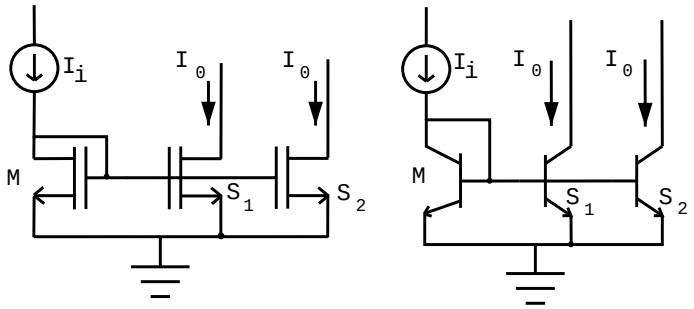

Figure 11: The Current Mirror - MOSFET and BJT implementations

Defining $\Delta V_T = \mathrm{V}_{TM}$ - V_{TS}, we can rearrange terms in the above equation to obtain

$$(\Delta V_T)^2 + \frac{2I_i}{k_M} + 2\sqrt{2I_i}k_M\Delta V_T = \frac{2I_0}{k_S} \tag{44}$$

We then have

$$\frac{I_0}{I_i} = \frac{k_S}{k_M} + \frac{k_S}{2}\frac{(\Delta V_T)^2}{I_i} + \sqrt{\frac{2}{k_M I_i}}\Delta V_T k_S \tag{45}$$

$$= \frac{\left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_M} + \frac{k_S}{2}\frac{(\Delta V_T)^2}{I_i} + \sqrt{\frac{2}{k_M I_i}}\Delta V_T k_S \tag{46}$$

In addition, errors will also arise due to channel-length modulation. We can conclude that the dominant effects that cause mismatch in current are the mismatches in the drain-source voltage, and the mismatch in the threshold voltage, V_T. Let us now consider the BJT realization of the same circuit (figure 11).

In this case, the difference between the input and output currents is caused by the finite current-gain. The input current-source, I_i has to supply the base current of the *master* BJT as well as the base current of all the *slave* BJTs. Assuming that there are n *slaves* connected to the master and further assuming that the emitter area is the same for all the transistors, we have

$$I_{CM} = I_i - \frac{n \cdot I_i}{\beta} \quad (47)$$

$$I_0 = I_{CM} \quad (48)$$

$$= I_i - \frac{n \cdot I_i}{\beta} \quad (49)$$

$$\frac{I_0}{I_i} = 1 - \frac{n}{\beta} \quad (50)$$

The mismatch in the current gain, β, between the transistors is a second-order effect and is not considered here. As the number of *slave* BJTs increases, the mismatch in current between the input and output increases. With BJTs, this places an upper bound on the number of *slaves* that can be connected to the *master*. In addition, errors will also be produced due to a) mismatch in V_{ce} and b) device sizes. The derivation is conceptually simple, and left to the reader as an exercise.

2.3 Current Mirror as a Current Amplifier

The Current Mirror's application is not limited to just mirroring the dc current required to bias the various transistors. The concept can be used to realize a current amplifier as shown in figure 12.

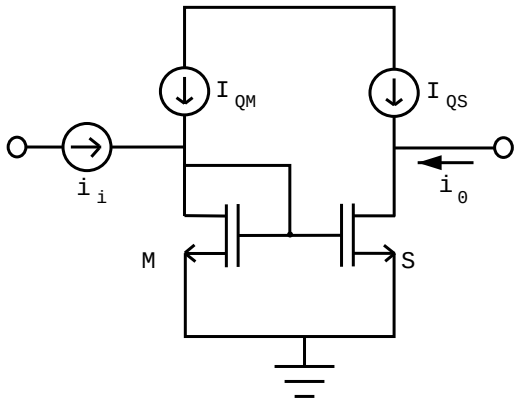

Figure 12: The Current Mirror as a Current Amplifier

We will make the following assumptions

$$\frac{\left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_M} = A_I \quad (51)$$

$$\lambda_M = \lambda_S \quad (52)$$

$$\Delta V_T = 0 \quad (53)$$

Using the above assumptions in equation 46, we have

$$\frac{I_{DS}}{I_{DM}} = \frac{\left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_M} \quad (54)$$

$$I_{DS} = I_{DM} \cdot A_I \quad (55)$$

We will now analyze what happens when a bidirectional signal current, i_i, is injected at the input of the current mirror. If i_0 is the resulting output signal current, we can write

$$I_{QS} + i_0 = A_I \left(I_{QM} + i_i\right) \quad (56)$$

If we now choose the bias currents, I_{QS} and I_{QM}, such that $I_{QS} = A_I I_{QM}$, equation 56 reduces to

$$i_0 = A_I \cdot i_i \quad (57)$$

i_i generates an input incremental change of voltage, v_i, equal to $\frac{i_i}{g_{mM}}$ around the quiescent dc voltage of $V_T + \sqrt{\frac{2I_M}{k_M}}$. This in turn generates an output current change around I_{QS} of $\frac{g_{mS}}{g_{mM}} i_i$ where,

$$\frac{g_{mS}}{g_{mM}} = \frac{k_S \left(V_{GSS} - V_T\right)}{k_S \left(V_{GSS} - V_T\right)} = \frac{k_S}{k_M} = A_I \quad (58)$$

This is an amplifier which is externally linear and internally non-linear. Current at the input is converted into a voltage (square-root of current). The voltage is then converted into current (square of voltage). Hence, the dynamic range over which the linear relationship is valid is very wide.

With BJTs, signal data is compressed first and then expanded. The BJT and MOSFET realizations are called log-domain amplifiers and square-root amplifiers, respectively. Such circuits are also called *Translinear Networks* since they are externally linear (I_0 vs. I_i) but internally non-linear. We will study them in more detail later in this chapter.

2.4 Current Mirror as a Current-Controlled Current Source

An ideal current-controlled current-source has zero input-impedance and high output-impedance. The current-mirror circuit has an input impedance of $\frac{1}{g_m}$ (refer figure 9) and an output impedance of r_{ds}. To make it a better current source, we need to increase the output impedance. In this section, we will discuss techniques that enhance the output impedance of the current-mirror.

One way to look at the output impedance is to view it as a dependence of the output current on the drain-source voltage. The output resistance will be much higher if we build a current mirror whose V_{DS} is maintained at the same value as that of the master and then pumping the output current of the *slave* into a common-gate MOSFET as shown in figure 13.

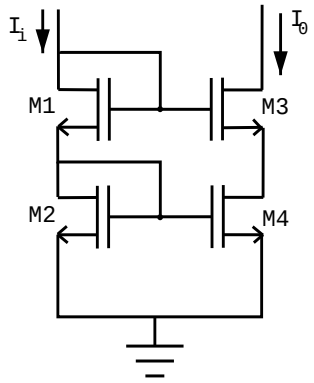

Figure 13: The Cascode Current Mirror

In this arrangement, the current I_0 is less dependent on the output voltage than in the previous one. In other words, the output impedance is higher ($r_0 = g_m r_{ds}^2$) This circuit is known as the cascode current mirror. Let us see how the drain-source voltage of the *slave* transistor is maintained the same as the drain-source voltage of the *master*.

Assuming that all devices have the same W/L, we can write

$$V_{G-M3} = V_{GS-M1} + V_{GS-M2} \quad (59)$$

$$= V_{GS-M3} + V_{DS-M4} \quad (60)$$

Since all the devices are equal in size, and further since the currents are equal, we can expect all the gate-source voltages to be equal (to first-order). Hence, from equations 59 and 60 we can write

$$V_{DS-M4} = V_{GS-M2} = V_{DS-M2} \tag{61}$$

We have assumed so far that all the transistors are in the saturation region. Hence, this circuit will behave as expected only if we ensure that each transistor has enough drain-source voltage to pinch-off the channel. For the simple current mirror of figure 11,

$$V_{DS} \geq V_{GS} - V_T \tag{62}$$

If we define V_{GS} - $V_T = \epsilon$, the simple current mirror will work as long as

$$V_{DS} \geq \epsilon \tag{63}$$

For the cascode current mirror to behave as expected, we need to provide the drain-source voltages for both M3 and M4. We know that $V_{DS-M4} = V_{GS-M2}$ (equation 61). V_{DS-M3} has to be sufficient to ensure that M3 is in the saturation region. Therefore,

$$\begin{aligned} V_{0min} &= 2V_{GS} - V_T & (64) \\ &= V_T + 2\epsilon & (65) \end{aligned}$$

Such a cascode current source can only work with a limited dynamic range for the output voltage. This restriction arises because the bottom transistors (M2 and M4) have more drain-source voltage than is required to pinch-off the channel. A higher dynamic range is hence obtained by ensuring that each transistor has a $V_{DS} = \epsilon$ as shown in figure 14. M5 and I' should be chosen such that the $V_{G-M1} = V_T + 2\epsilon$.

Based on our discussion of current-mirrors so far, we can conclude that

[1]. Current mirrors can be used as *active loads* to simulate high impedances at a given current with low dc voltage drops (nϵ)

[2]. Current mirrors can act as biasing circuits sourcing or sinking a given current

[3]. Current mirrors can also be used as current amplifiers or current-controlled current sources

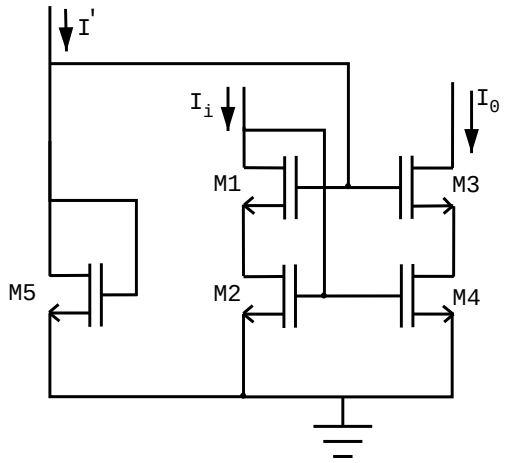

Figure 14: Cascode Current Mirror with High Dynamic Range

2.5 Supply-Independent Current Source

In the earlier sections in this chapter, we discussed mirroring-circuits that can be used to bias the active devices in a circuit. The dependence of the bias current on the supply voltage in the *slave* transistors is equal to the dependence of the bias current on the supply voltage in the *master* transistor. In other words, the mirrored-current can only be as insensitive to supply-voltage variations as the *master* current-source is. In this section, we will consider one example of a circuit that allows for the generation of a bias-current that is insensitive to supply-voltage variations.

We know that a diode-connected MOS transistor develops a gate-source voltage equal to $V_T + \sqrt{\frac{2I}{k_0 \frac{W}{L}}}$. This voltage is used to bias another n-channel MOSFET (size: $n\frac{W}{L}$) whose source is degenerated using a resistor, R. Let us further assumes that the same current, I, flows through both the transistors.

We can then write,

$$V_{GS1} = V_T + \sqrt{\frac{2I}{k_0 \frac{W}{L}}} \tag{66}$$

$$V_{GS2} = V_T + \sqrt{\frac{2I}{k_0 n \frac{W}{L}}} \tag{67}$$

$$V_{GS1} = V_{GS2} \tag{68}$$

$$I = \frac{\sqrt{\frac{2I}{k_0 \frac{W}{L}}} - \sqrt{\frac{2I}{k_0 n \frac{W}{L}}}}{R} \tag{69}$$

$$\sqrt{I} = \left[\frac{\sqrt{\frac{2}{k_0 \frac{W}{L}}} - \sqrt{\frac{2}{k_0 n \frac{W}{L}}}}{R} \right] \tag{70}$$

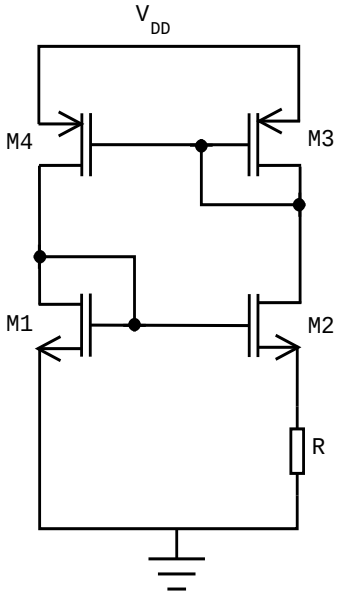

Figure 15: Supply-Independent Current Source: $\left(\frac{W}{L}\right)_{M2} = n\left(\frac{W}{L}\right)_{M1}$; $\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4}$

From equation 70, we observe that the current, I, is independent of the supply voltage. All the transistors biased with this control-voltage will have

a g_m that depends only on $\frac{W}{L}$ and R, and is insensitive to supply-voltage variations. The circuit is shown in figure 15.

This technique can be used in biasing op-amp stages. Since the current, mI,(where m is the ratio in $\frac{W}{L}$ between the *master* and the *slave*) and g_m are insensitive to supply-voltage variations, the circuit will exhibit a very good power-supply rejection-ratio (PSRR). The current is also independent of the threshold voltage, V_T. We will use this biasing technique in the subsequent chapters when we discuss design of op-amps.

3 Translinear Networks

3.1 The Translinear Principle

We had provided a brief description of translinear networks in the section on using current-mirrors as current amplifiers. Figure 16 shows the basic current-mirror circuit.

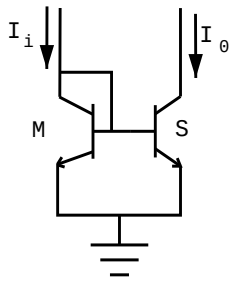

Figure 16: The Translinear Network

Here, I_i generates a V_{BE} across the *master* given by

$$V_{BEM} = V_t \ln \frac{I_i}{I_{s0-M}} = V_{BES} \tag{71}$$

This voltage generates a collector current in the *slave* BJT given by

$$I_0 = I_{s0-S} e^{\frac{V_{BES}}{V_t}} \tag{72}$$

The relation between I_0 and I_i is given by

$$I_0 = \frac{A_{ES}}{A_{EM}} I_i \tag{73}$$

where we have assumed that the current density of the reverse saturation current is the same in the two devices.

We can extend this principle (with BJTs in particular) in the following manner. Consider 2n transistors whose base-emitter voltages are connected in a loop with n transistors in clock-wise direction and n transistors in anti-clockwise direction as shown in figure 17 (the order in which they appear does not matter).

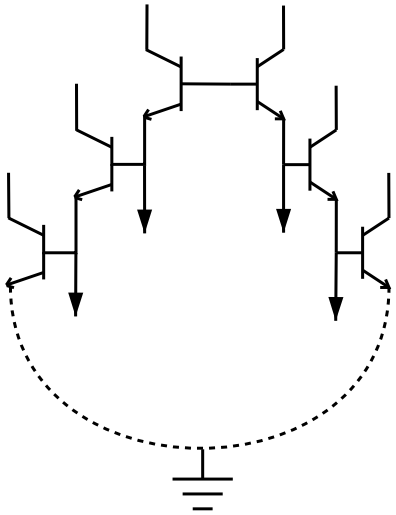

Figure 17: A Translinear Network with 2n BJTs

Then, using Kirchoff's loop equation, we can write

$$\sum_{i=1}^{n} V_{BEi} = \sum_{j=1}^{n} V_{BEj} \tag{74}$$

$$\sum_{i=1}^{n} V_t \ln \frac{I_{ei}}{I_{s0}} = \sum_{j=1}^{n} V_t \ln \frac{I_{ej}}{I_{s0}} \tag{75}$$

$$\sum_{i=1}^{n} \ln \frac{I_{ei}}{A_{ei}} = \sum_{j=1}^{n} \ln \frac{I_{ej}}{A_{e0}} \tag{76}$$

$$\prod_{i=1}^{n} J_{ei} = \prod_{j=1}^{n} J_{ej} \tag{77}$$

In words, one can express the relationship as *the product of emitter currents in the clockwise direction is equal to the product of emitter currents in the anti-clockwise direction*

One should note that the circuit fundamentally still remains a current-controlled current-source; the main difference now is that there are multiple controlling inputs. Let us now consider some examples. We will start with the current mirror of figure 16.

$$J_{eS} = J_{eM} \tag{78}$$

$$\frac{I_{eS}}{A_{eS}} = \frac{I_{eM}}{A_{eM}} \tag{79}$$

$$I_{eS} = \frac{A_{eS}}{A_{eM}} I_{eM} \tag{80}$$

Figure 18 shows the cascode current mirror. One can view this circuit as a translinear circuit in a 4 transistor loop.

From equation 77, we can write,

$$J_{eS}^2 = J_{eM}^2 \tag{81}$$

$$\frac{I_{eM}}{A_{eM1}} \cdot \frac{I_{eM}}{A_{eM2}} = \frac{I_{eS}}{A_{eS1}} \cdot \frac{I_{eS}}{A_{eS2}} \tag{82}$$

$$I_{eS} = \sqrt{\frac{A_{eS1} A_{eS2}}{A_{eM1} A_{eM2}}} I_{eM} \tag{83}$$

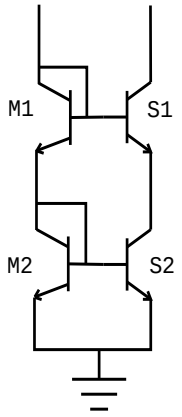

Figure 18: Cascode Current Mirror - Translinear Network with 4 Transistors

3.2 Applications of Translinear Networks

Figure 19 shows the squarer circuit. The equations that describe the behaviour of this circuit are given below.

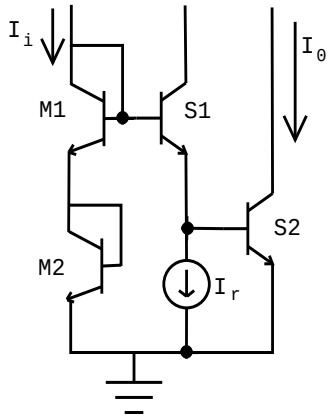

Figure 19: Squaring Circuit

$$I_i^2 = I_r \cdot I_0 \tag{84}$$

$$I_0 = \frac{I_i^2}{I_r} \tag{85}$$

Figure 20 shows a circuit that can be used either as a multiplier or a divider. The equations are described below.

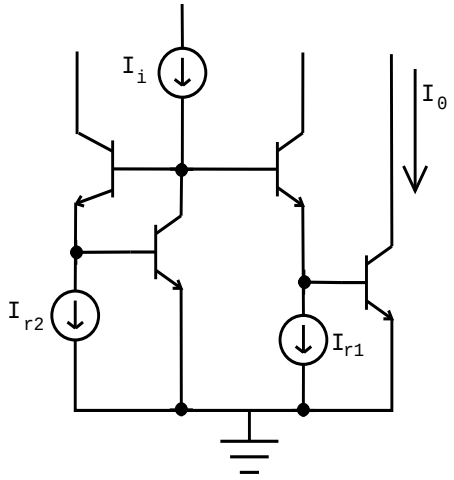

Figure 20: Divider and Multiplier Circuit

$$I_i \cdot I_{r2} = I_{r1} \cdot I_0 \tag{86}$$

$$I_0 = \frac{I_i \cdot I_{r2}}{I_{r1}} \tag{87}$$

In equation 87, if we choose $I_i = I_{i1}$ and $I_{r2} = I_{i2}$, and I_{r1} to be a reference current, we will obtain a multiplication of the two input currents, I_{i1} and I_{i2}.

$$I_0 = \frac{I_{i1} \cdot I_{i2}}{I_{r1}} \tag{88}$$

If instead, we choose $I_i = I_{i1}$ and $I_{r1} = I_{i2}$, and I_{r2} to be a reference current, we will obtain a division of the two input currents, I_{i1} and I_{i2}.

$$I_0 = \frac{I_{i1}}{I_{i2}} \cdot I_{r2} \tag{89}$$

Figure 21 shows the square-rooting circuit; the equations are described below.

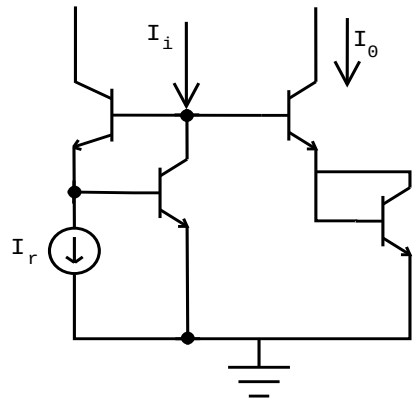

Figure 21: Square Rooting Circuit

$$I_i I_r = I_0^2 \tag{90}$$
$$I_0 = \sqrt{I_i I_r} \tag{91}$$

Example 1 *Design a Translinear Circuit that can realize the sum of squares of two input currents.*

Figure 22 shows the circuit that can realize the sum of squares of two input currents. The equations that govern the behaviour of this circuit are described below.

$$I_a^2 = I_1 (I_1 + I_2) \quad TLL\ 1 \tag{92}$$
$$I_b^2 = I_2 (I_1 + I_2) \quad TLL\ 2 \tag{93}$$
$$I_a^2 + I_b^2 = (I_1 + I_2)^2 \tag{94}$$
$$= I_c^2 \tag{95}$$
$$I_c = \sqrt{I_a^2 + I_b^2} \tag{96}$$

The reader is referred to [4] for a number of other examples of translinear networks.

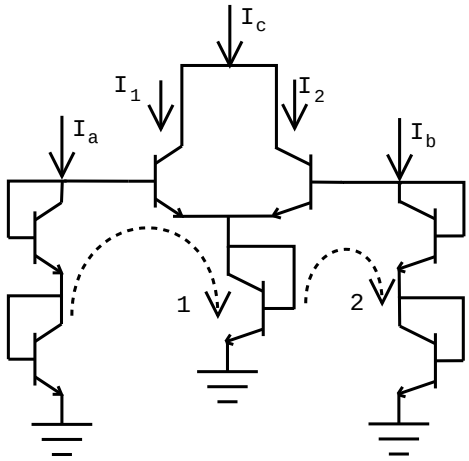

Figure 22: A Circuit That Realizes Sum of Squares

3.3 Gilbert's Gain Cell

In this section, we will consider an application of translinear networks that has found widespread application in analog ICs. The original circuit (and quite a few of its derivatives) was conceived by B. Gilbert[3], and hence the name for this gain-cell.

Consider the circuits shown in figure 23.

Using the translinear principle, we can write

$$I_{e1}I_{e3} = I_{e4}I_{e2} \tag{97}$$

$$\frac{I_{e1}}{I_{e2}} = \frac{I_{e4}}{I_{e3}} \tag{98}$$

$$\frac{I_{e1} - I_{e2}}{I_{e1} + I_{e2}} = \frac{I_{e4} - I_{e3}}{I_{e4} + I_{e3}} \tag{99}$$

If we define $\mathrm{I}_{e1} = \frac{I_{00}}{2} + \frac{\Delta I_i}{2}$, and $\mathrm{I}_{e2} = \frac{I_{00}}{2} - \frac{\Delta I_i}{2}$, we can rewrite equation 99 as

$$\frac{\Delta I_i}{I_{00}} = \frac{\Delta I_0}{I_{00}} \tag{100}$$

$$\Delta I_0 = \left(\frac{I_{01}}{I_{00}}\right) \Delta I_i \tag{101}$$

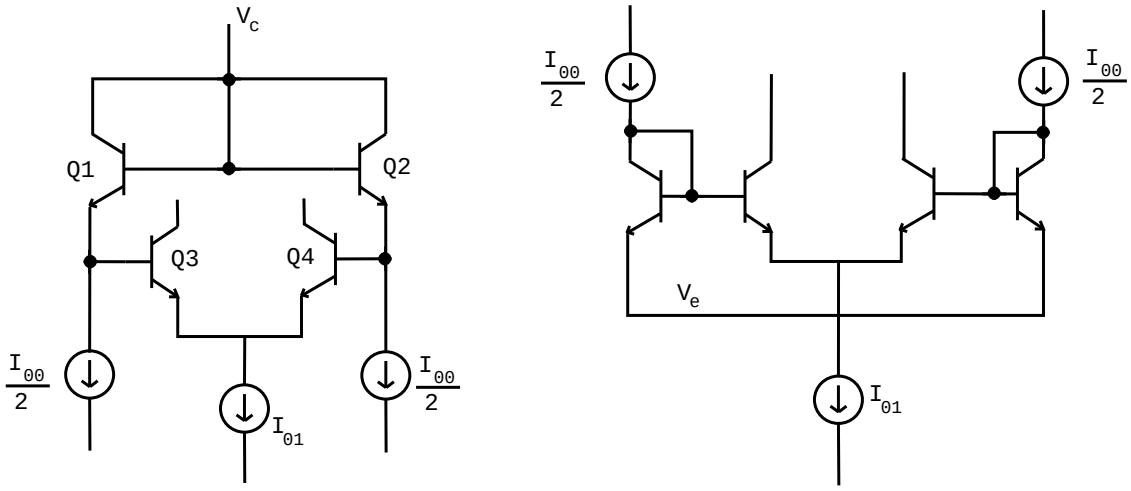

Figure 23: The Gilbert's Gain Cell

In other words, the circuit describes a differential current amplifier. One can stach such cells one over the other with the successive stages operating at higher current. This can be used to obtain gain which is a ratio of dc operating currents. If these dc currents are obtained using current-mirrors, the gain can be expressed as a ratio of device areas. This structure is a wideband structure without feedback that gives linear current amplification over a wide dynamic range without distortion. We will use this idea later in designing precision voltage multipliers with wide dyanmic range using linear differential transconductors.

4 Diode Connected Transistor as Current Feedback Structures

Figure 24 shows an open-loop current amplifier. The input and output currents are related by $I_0 = \beta I_i$. When the loop is closed as shown in figure 25, the system transfer function is given by

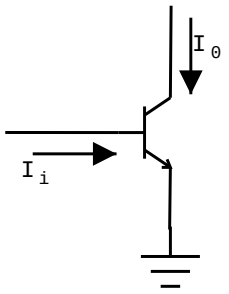

Figure 24: Current Amplifier - Open Loop

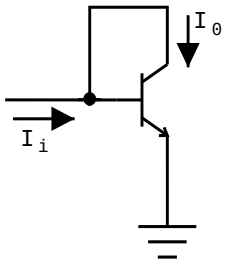

Figure 25: Current Amplifier - Closed Loop

$$\beta\,(I_i - I_0) = I_0 \tag{102}$$

$$\frac{I_0}{I_i} = \frac{\beta}{\beta+1} = \alpha \tag{103}$$

This is the technique of pumping a fixed current into the collector of a transistor. The base-emitter voltage adjusts itself to accomodate this current through the transistor. This can be achieved better in the case of a MOSFET since the open loop gain is ∞. The MOSFET open-loop and closed-loop current amplifier are shown in figure 26.

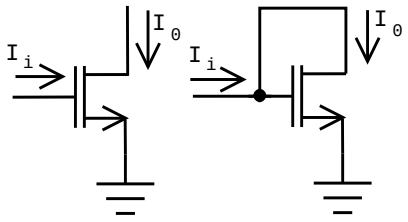

Figure 26: Current Amplifier - MOSFET implementation

As the open loop current-gain $\rightarrow \infty$, $\frac{I_0}{I_i} \rightarrow 1$. The error current, I_i - I_0, tends to zero. In this case, the gate-source voltage will adjust itself to permit the flow of drain current.

The two basic structures that we discussed were derived out of common-emitter and common-source amplifiers, and are respectively known as common-base and common-gate amplifiers. Both these circuits are near-ideal CCCS with a gain of unity. These are wideband because they are negative feedback structures ($\beta f_\beta = \alpha f_\alpha = f_\tau$). The current gain-bandwidth product remains the same, and hence, a unity gain current amplifier will have a very high bandwidth.

To increase the forward loop gain, we can cascade two current amplifiers in the forward path. Two configurations are possible with this idea and both are shown in figure 27.

The same idea can be extended to BJTs as well. The configurations are shown in figure 28.

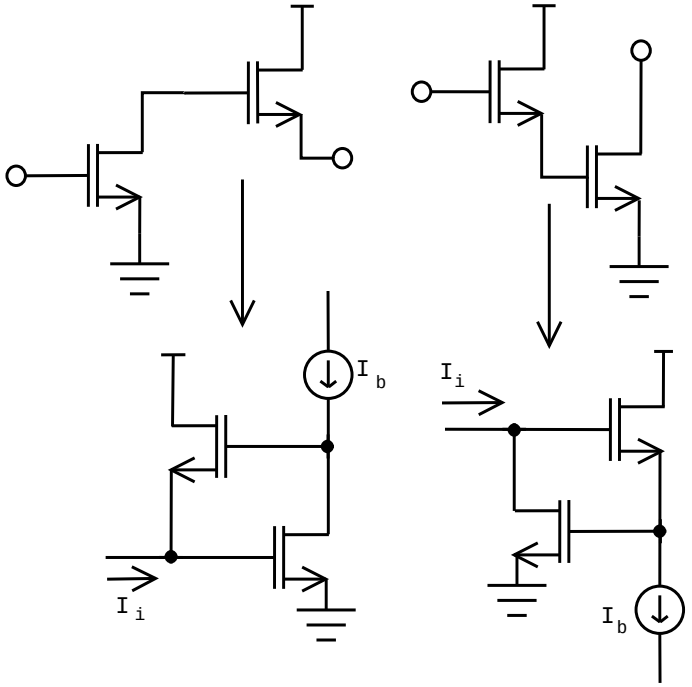

Figure 27: Possible Configurations with Two Current Amplifiers in the Forward Path - MOS implementations

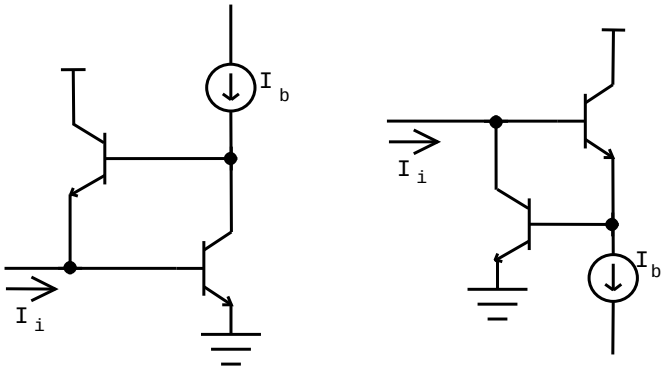

Figure 28: Possible Configurations with Two Current Amplifiers in the Forward Path - BJT implementations

4.1 Wilson Current Mirror as a Current-Feedback Structure

Figure 29 shows the BJT implementation of a Wilson's current mirror. The following equations analyze this circuit as a current-feedback structure.

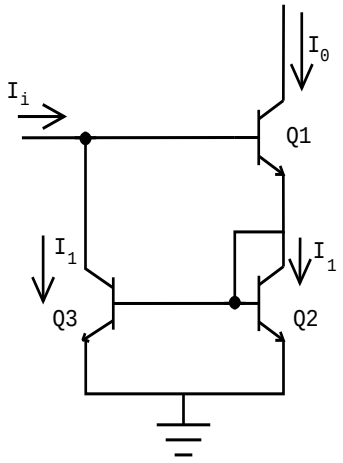

Figure 29: Wilson Current Mirror - BJT implementation

Relating the collector and base currents in Q1, we have

$$I_0 = \beta\left(I_i - I_0\right) \tag{104}$$

Relating the emitter and collector currents in Q1, we have

$$\begin{aligned} I_0 &= \frac{\beta}{\beta+1} \cdot I_1 \cdot \left(1 + \frac{2}{\beta}\right) && (105) \\ &= I_1 \cdot \frac{\beta+2}{\beta+1} && (106) \end{aligned}$$

Substituting equation 106 in equation 104, we have

$$\begin{aligned} \frac{I_0}{I_i} &= \frac{1}{1 + \frac{2}{\beta(\beta+2)}} && (107) \\ &= \frac{1}{1+g_l} && (108) \end{aligned}$$

where the loop gain, g_l, is given by

$$g_l = \frac{\beta\,(\beta + 2)}{2} \tag{109}$$

In an ordinary current mirror, the loop gain, g_l, is equal to $\frac{\beta}{2}$. Due to increased current feedback, the output resistance is increased from r_{ce} to $\frac{\beta r_{ce}}{2}$. It should be noted that in the case of a cascode current mirror, the output resistance is βr_{ce}

Another point that merits mention here is that while the Wilson current mirror uses current-feedback, the Cascode current mirror uses voltage-feedback. We will study this in more detail when we discuss transistor realizations of feedback amplifiers in the following chapter.

Current mirroring in the Wilson mirror will be exact if both the transistors are maintained to have the same V_{ce}; this is made possible by introducing a diode(Q_4) at the summing node as shown in figure 30

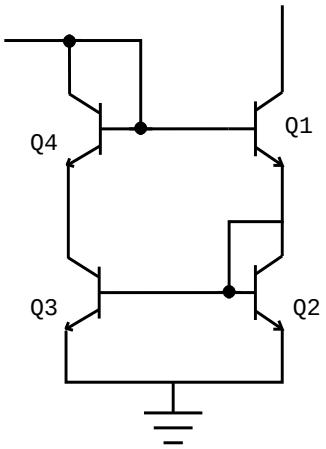

Figure 30: Wilson Current Mirror with Exact Mirroring

The same circuit can be realized, if required, using MOS transistors as well and is shown in figure 31. It must be noted, though, that the Wilson current-mirror hardly finds any use in MOS ICs. Since the dc current-gain of a MOS transistor is ∞, one obtains little benefit by using techniques that enhance the loop gain.

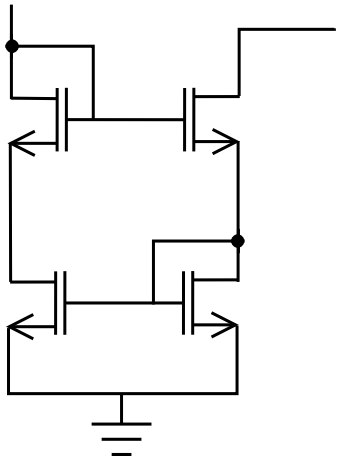

Figure 31: Wilson Current Mirror - MOS implementation

4.2 Other Applications of Current-Feedback Structures

Current-feedback can be used in other applications as well, and one such example is discussed here. Since the ICs we design are used in a number of various real-life situations, it is required that they be protected against electro-static discharges (ESD). In other words, the circuit should be able to withstand a sudden impulse in current at its input terminals. If we do not use a protection circuit, the current will flow into the base of the input transistor, and might result in device-breakdown. The circuit will then lose its functionality, and render the system that it is housed in useless.

We will now consider a protection circuit that uses current-feedback. Consider the circuit shown in figure 32.

In figure 32, Q1 is the input transistor to be protected. Let us further assume that R is the biasing resistor used for the circuit. In the absence of BJT Q2, the current will flow into the base of Q1 and degrade permanently, or breakdown, the device. By introducing transistor Q2, we create a feedback loop that ensures that the collector current of Q2 *follows* the input current. As long as Q2 is capable of sustaining the impulse current, the circuit will behave correctly for a subsequent input signal. Other than introducing a parasitic capacitance at the input node, Q2 does not affect the response of the circuit to a voltage input.

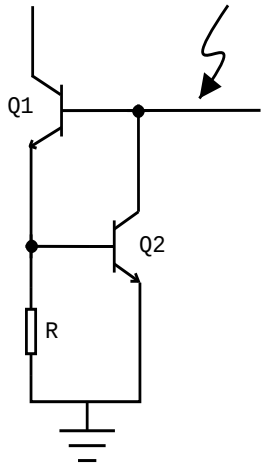

Figure 32: Protection Circuit - BJT implementation

5 Voltage Sources and Voltage References

Voltage sources (secondary power supplies and level shifters) are needed for baising the active devices inside the IC. A well designed voltage source will have an output that is independent of the primary bias voltage (good line regulation characteristic). Further, the source should be able to deliver load current without any change in output voltage (good load regulation characteristic). A low output resistance is also required for a voltage source so that systems that use a common voltage source are not coupled to each other.

Let us begin by considering diode-connected transistors. A diode connected MOS transistor, biased at a drain current of I_D, develops a gate-source voltage given by $V_{GS} = V_T + \sqrt{\frac{2I_D}{k}}$, while a diode connected BJT, biased at an emitter current of I_e, develops a base-emitter voltage given by $V_{BE} = V_t \ln \frac{I_e}{I_{e0}}$. These voltages have a negative temperature co-efficient and at a given current, the variation of output voltage is linear with respect to temperature. Hence, this can be used as a temperature transducer or sensor. The output resistance in both cases can be shown to be $\frac{1}{g_m}$ where g_m is the transconductance at the operating current.

A string of n such diodes can give nV_γ and nV_T for BJTs and MOS transistors, respectively.

The diode connected BJT has a voltage V_{BE} of ≈ 0.6V, and a temperature

co-efficient of -2mV/^{o}C. Consider two such diodes operating at two different currents I_1 and I_2. The respective base-emitter voltages in the two transistors are $V_t \ln \frac{I_1}{I_{e0}}$ and $V_t \ln \frac{I_2}{I_{e0}}$.

If the difference voltage between the two diodes is considered (as shown in figure 33,

$$V_0 = V_{BE1} - V_{BE2} \tag{110}$$

$$\Delta V_{BE} = V_t \ln \frac{I_1}{I_{e0}} - V_t \ln \frac{I_2}{I_{e0}} \tag{111}$$

$$= V_t \ln \frac{I_1}{I_2} \tag{112}$$

$$= \frac{kT}{q} \ln \frac{I_1}{I_2} \tag{113}$$

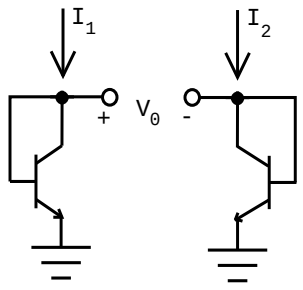

Figure 33: Diode-connected BJT as a Voltage Source

The output voltage is independent of the reverse saturation current, I_{e0}. Since $\frac{kT}{q}$ is precisely known (26mV at 300K), the output voltage of this current is precisely known for a given current ratio $\left(\frac{I_1}{I_2}\right)$. Its temperature co-efficient is positive and is nearly an absolute constant given by $\frac{k}{q} \ln \frac{I_1}{I_2}$.

Such a source can hence be used for precision temperature measurement or sensing.

5.1 Voltage References

In the previous section, we discussed circuits that provide an output voltage with positive and negative temperature co-efficients. We can combine the

two circuits to obtain a *voltage reference* with zero temperature co-efficient. Such references are used in A/D converters and the accuracy of the conversion depends on the accuracy of the reference voltage.

Reference sources are required to maintain a voltage that is independent of the primary bias voltage as well as be independent of temperature. They are not to be loaded and therefore the output impedance need not be low.

One example of a voltage reference is described below. Consider the circuit shown in figure 34.

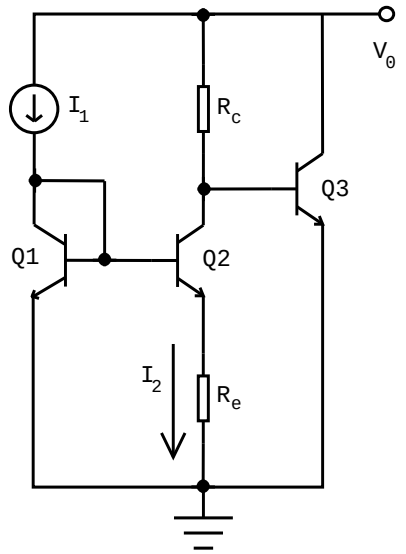

Figure 34: BJT Voltage Reference

We will now compute the output voltage of this reference circuit. We will begin by expressing the different base-emitter voltages as a function of their respective emitter currents.

$$
\begin{aligned}
V_{BE1} &= V_t \ln \frac{I_1}{I_{e0}} && (114)\\
V_{BE2} &= V_t \ln \frac{I_2}{I_{e0}} && (115)\\
V_{BE1} - V_{BE2} &= \Delta V_{BE} && (116)\\
&= V_t \ln \frac{I_1}{I_2} && (117)\\
I_2 = \frac{\Delta V_{BE}}{R_e} &= \frac{V_t}{R_e} \ln \frac{I_1}{I_2} && (118)\\
I_2 R_c &= \frac{R_c}{R_e} V_t \ln \frac{I_1}{I_2} && (119)\\
V_0 &= V_{BE3} + \frac{R_c}{R_e} V_t \ln \frac{I_1}{I_2} && (120)
\end{aligned}
$$

If we define n = $\frac{R_c}{R_e}$, we can rewrite equation 120 as

$$
\begin{aligned}
V_0 &= V_{BE3} + n \ln \frac{I_1}{I_2} V_t && (121)\\
&= V_{BE3} + n \Delta V_{BE} && (122)
\end{aligned}
$$

Since we require a reference that is independent of temperature,

$$
\begin{aligned}
\frac{\partial V_0}{\partial T} &= 0 && (123)\\
\frac{\partial V_{BE}}{\partial T} + n \frac{\partial \Delta V_{BE}}{\partial T} &= 0 && (124)\\
n = \frac{\frac{-\partial V_{BE}}{\partial T}}{\frac{\partial \Delta V_{BE}}{\partial T}} &= \frac{2}{\frac{V_t}{T} \ln \frac{I_1}{I_2}} && (125)\\
&= \frac{2}{\frac{25}{300} \ln \frac{I_1}{I_2}} && (126)\\
&= \frac{24}{\ln \frac{I_1}{I_2}} && (127)
\end{aligned}
$$

We can rewrite equation 127 as

$$n \ln \frac{I_1}{I_2} = 24 \tag{128}$$

Substituting equation 128 in equation 121, we have

$$\begin{aligned} V_0 &= V_{BE3} + 24V_t & (129)\\ &\approx 0.6 + 24 \times 25 & (130)\\ &\approx 1.2 \text{ V} & (131) \end{aligned}$$

We could have fixed I_1 in this circuit by using a pull-up resistor, R_1. In such a scenario, equation 121 will reduce to

$$V_0 = V_{BE3} + nV_t \ln \frac{R_c}{R_1} \tag{132}$$

5.2 Supply-Independent Voltage Sources

In the preceding section, we realized voltage sources and voltage references by using a bias current to develop a voltage across a diode-connected transistor. In such circuits, the dependence of the bias-current on the supply voltage dictates the dependence of the output voltage on the supply voltage. In order to obtain an output voltage that is independent of the supply voltage, we need a bias current that is independent of supply voltage. This will be possible only if we use a device that can generate a current with zero control voltage.

One such device where the channel exists at zero V_{GS} is the depletion-mode MOSFET. A depletion-mode MOSFET or JFET with the gate and source shorted can offer a current independent of supply voltage without using a resistance as long as we ensure that $|V_{DS}| > |V_P|$. The only disadvantage is that the current, I_{DSS}, is not exactly known. This current can pass through a diode connected MOS ($V_T + \epsilon$) which can be used as a voltage source. This node cannot be loaded and hence, we need to include a buffer stage as well. The final circuit is shown in figure 35. The reader is referred to [5] for more examples. Some of them are provided here as exercises for the reader.

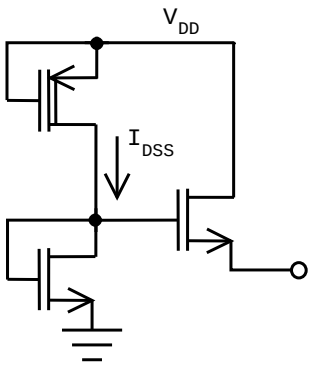

Figure 35: Supply-Independent Voltage Source

6 Summary - Biasing Devices Like BJTs and MOSFETs

BJTs and MOSFETs, when used as amplifying devices in circuits, must remain in the active region. BJTs, for example, must have the base-emitter junction forward-biased and the base-collector junction reverse-biased as long as the signal exists. The channel in a MOSFET must stay pinched-off close to the drain end as long as the signal exists.

This can be done using two methods: We can either fix the quiescent input voltage or fix the quiescent output current. Fixing the output current by fixing the emitter current in BJTs is the *most stable* way of biasing. This will ensure that the bias on the active device is insensitive to device parameters. In a similar fashion, fixing the output current by fixing the source current is the most stable form of biasing a MOSFET in the active region. Fixing the bias current in a BJT by using either a base current or a base-emitter voltage makes the output current dependent on device parameters, and is hence not advised.

We can use what we have learnt on current-mirrors to fix the bias currents in circuits. In its simplest form, a diode-connected transistor can be used to develop the voltage required to bias at a certain current, and use this control voltage to reflect the required current in the other devices. Other requirements such as output resistance might dictate use of the more complicated current-mirrors.

The collector-base reverse bias or the drain-gate bias required to maintain

the devices in active region can be applied through resistors connected to the supply voltage as shown in figure 36

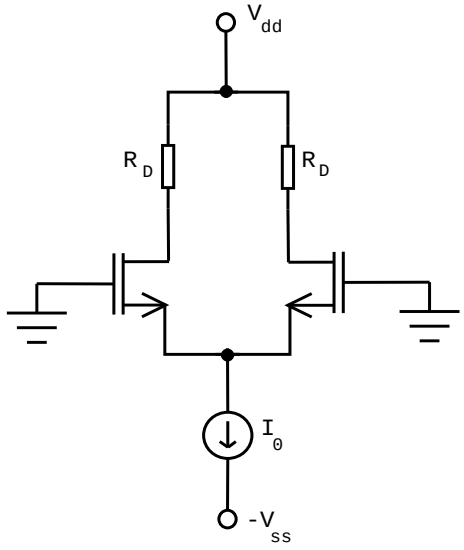

Figure 36: Method to Bias MOSFETs

We had mentioned earlier that, by virtue of their high output-impedances and low headroom-requirements, can be used as active loads. In such a scenario, we need to study other means of maintaining the drain-gate bias. We will revisit this problem when we study high-gain differential amplifiers.

7 Exercises

[1]. Using the circuit shown in figure 12, realize a CCCS with a gain of 10. The circuit should handle an input signal current of 100μAsin(1000t). Sketch the output waveform and determine the bandwidth of this circuit in terms of g_m and C_{gs}

[2]. For the circuit shown in figure 37, compute the collector current through transistor Q2. Assume that the emitter junction-area of Q2 is twice the emitter junction-area of Q1. Will the collector current in Q2 change if we remove the 1KΩ resistor and connect the emitter of Q1 to ground instead? If so, what will the new collector current in Q2 be?

[3]. Show that the circuit shown in figure 38 generates a low-valued current. Derive the expression for the collector current through Q2

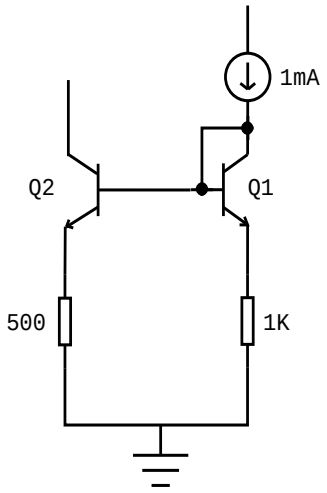

Figure 37: Figure for Problem 2

[4]. Use the translinear principle to prove that the circuit shown in figure 39 behaves as a signal normalizer. In other words, show that the following relation is satisfied.

$$I_k^{'} = \frac{I_k}{\sum_{k=1}^{n} I_k} I_e$$

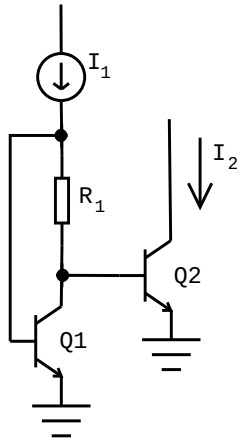

Figure 38: Figure for Problem 3

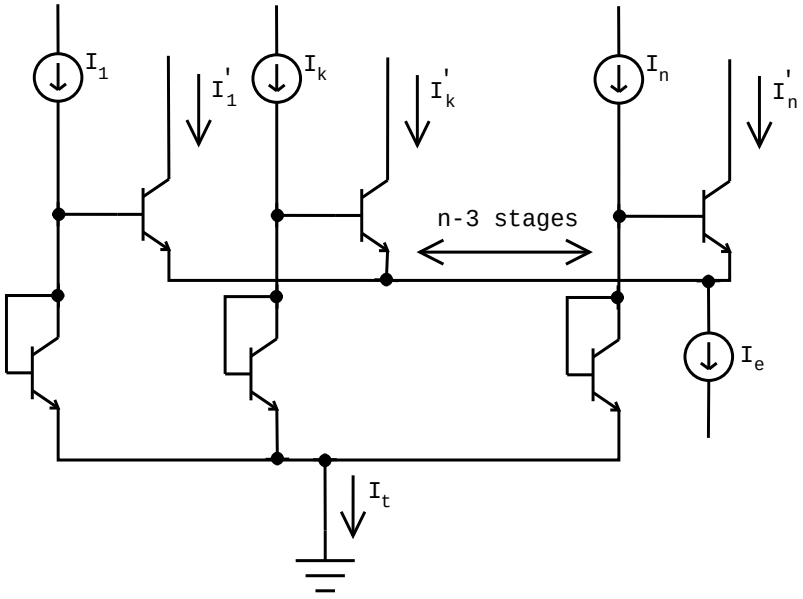

Figure 39: Figure for Problem 4

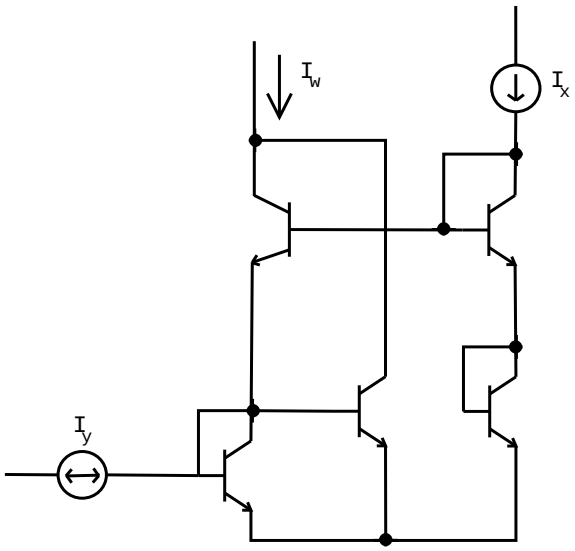

Figure 40: Figure for Problem 5

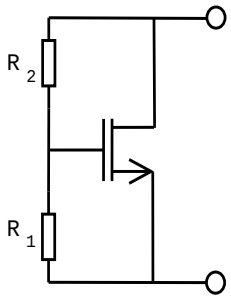

Figure 41: Figure for Problem 9

[5]. Use the translinear principle to relate I_w to I_x and I_y for the circuit shown in figure 40

[6]. Design a current mirror using p-channel MOSFETs to source 100μA current. Modify the simple current mirror into a) a cascode current mirror and b) high dynamic-range, high-output resistance current mirror

[7]. Show that the output impedance of the cascode current mirror is $g_m r_{ds}$ times the output impedance of the simple current mirror. Simulate the current mirrors and compare their characteristics (Plot V_0 vs. I_0 for different values of I_i)

[8]. Derive the expression for output resistance for the MOSFET-based Wilson's current mirror shown in figure 31. Express the result in terms of the small signal parameters of the transistors

[9]. Show that the voltage source shown in figure 41 can generate a voltage equal to $V_T\left(1+\frac{R_2}{R_1}\right)$ with an output resistance of $\frac{1}{g_m}\left(1+\frac{R_1}{R_2}\right)$. If this simulates a zener diode of $V_T\left(1+\frac{R_2}{R_1}\right)$, what is its knee current?

[10]. For the circuit shown in figure 42, derive an expression for the output voltage. Transistor Q1 has an emitter area of A_0, while transistors Q2 and Q3 have emitter areas of nA_0. Note that this circuit realizes a bandgap voltage reference. Simulate the circuit as well, and plot the variation in output voltage as a function of temperature

[11]. Derive an expression for the output voltage for the circuit shown in figure 43. What is the effect of any offset on the input of the op-amp?

[12]. Consider the circuit shown in figure 44. Derive an expression for the output voltage. What is the effect of any offset at the input of the op-amp? What is the disadvantage of this circuit (hint: Can it self-bias?)

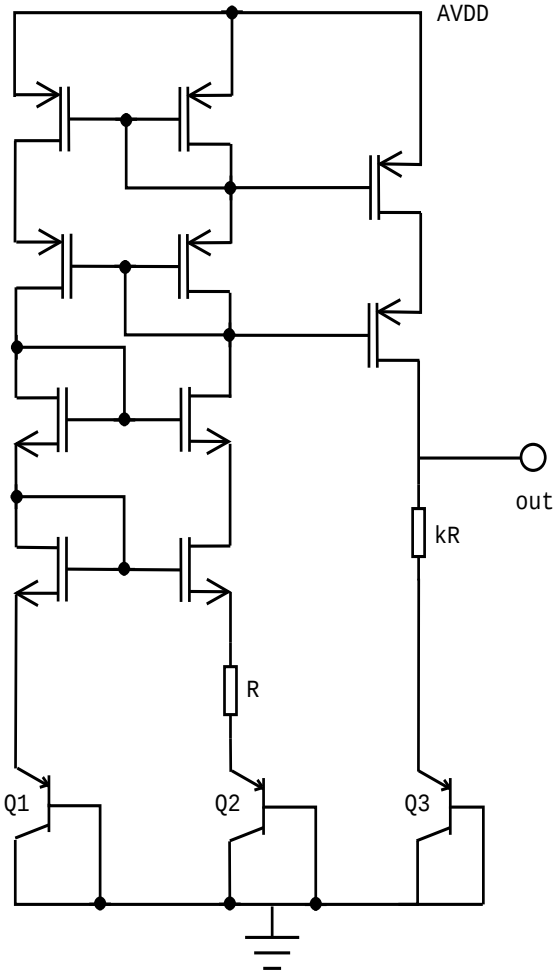

Figure 42: Figure for Problem 10

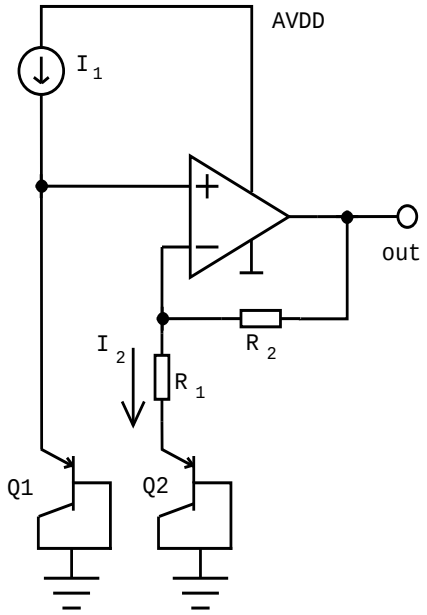

Figure 43: Figure for Problem 11

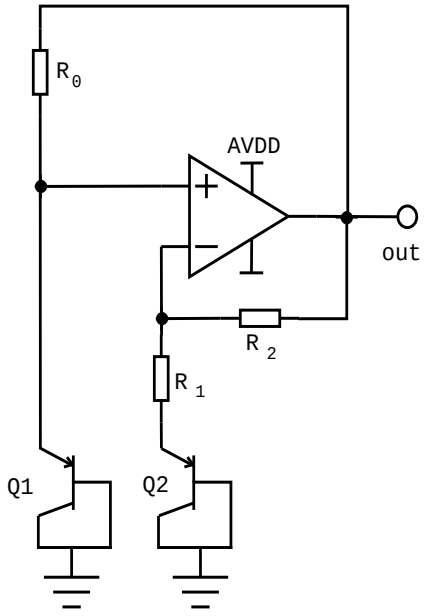

Figure 44: Figure for Problem 12

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