Chapter 1: Realization of IC Building Blocks Using Principles of Network Theory

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1 Introduction

The components that constitute an Integrated Circuit (IC) can be broadly classified into two types: Active and Passive. Any component that is capable of giving *power gain* is called 'Active'. Components that are incapable of giving power gain are classified as 'Passive'. Examples of Passive Elements are resistors, capacitors and inductors(including transformers). Diodes are also passive elements (there are some exceptions like tunnel diodes). Examples of Active Elements are Bipolar Junction Transistors (BJTs), Junction Field Effect Transistors (JFETs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Amplifiers (Amps) and Operational Amplifiers (Op-Amps)

2 The One-Port Network

Figure 1 shows a block diagram of a one-port or two-terminal signal processing element. The two variables that exist in such an element are the input voltage, v_i, and the input current, i_i. One of these can be chosen to be an *independent variable*; the other becomes a *dependent variable*. For e.g., if v_i is the independent variable, i_i, the current, becomes the dependent variable, and the relation between the variables is given by equation 1.

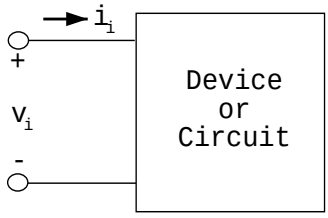

Figure 1: One-Port Signal Processing Element

$$i_i = G \cdot v_i (or) Y \cdot v_i \tag{1}$$

G and Y are called the *conductance* and *admittance*, respectively. Alternately, if i_i is chosen as the independent variable, v_i becomes the dependent variable, and the relation between the variables is given by equation 2.

$$v_i = R \cdot i_i (or) Z \cdot i_i \tag{2}$$

R and Z are called the *resistance* and *impedance*, respectively.

2.1 Passive Components

In an IC, resistance or conductance can be obtained by using diffused semiconductors. The dependence of the resistance on the physical dimensions, and the semiconductor properties is given in equation 3. This component dissipates power and is needed only for converting voltage to current or current to voltage.

$$R = \frac{\rho \cdot L}{A} = \frac{\rho \cdot L}{d \cdot W} = \frac{L}{d \cdot \sigma \cdot W}$$
$$R_{sq} = \frac{1}{\sigma \cdot d} \text{ ohm/sq.} \tag{3}$$

Capacitors and Inductors are passive elements that are preferred to resistors because they do not dissipate any power. Of these two, the capacitor is available as a Junction Capacitor, an Oxide Capacitor or as a Metal-Insulator-Metal(MIM) Capacitor.

The Oxide Capacitor exhibits higher density, while the MIM capacitors exhibit better linearity characteristics. These two types of capacitors are preferred over their junction counterparts. The relation between the value of capacitance, the physical dimensions and the insulator properties, are provided in equation 4. Since ϵ/d is a process parameter, the total capacitance is directly proportional to the area. Values in the range of a few pFs are common in ICs.

$$C = \frac{\epsilon \cdot A}{d} = \frac{\epsilon \cdot W \cdot L}{d} \tag{4}$$

Another aspect that needs to be considered in the realization of passives on ICs is the tolerance on absolute values. Both capacitors and resistors can vary by as much as 30%. As a result, it is preferred to realize most functions that are needed for signal processing as a ratio of similar elements. The tolerance on the ratio is typically an order of magnitude better than the tolerance on the absolute values.

Inductors are not easily fabricated in an IC planar technology. Only inductors of the order of a few nH have been realized. In addition, the quality

factor of these inductors is also low ($Q < 20$ for most Silicon-based implementations). The use of such inductors is limited to Radio Frequency(RF) circuits.

Theoretically, inductors are not necessary as signal processing elements because capacitors can perform the same functions of integrating and differentiating (described in equation 5) depending upon the choice of independent variable.

$$v = \frac{1}{C} \cdot \int i \cdot dt \text{ (integration)}$$
$$i = C \cdot \frac{dv}{dt} \text{ (differentiation)} \quad (5)$$

Diode (switch) is the other passive component required for signal processing. An ideal diode can be defined as a nonlinear device with two regions of operation: a *forward biased region* where the independent variable is i and the dependent variable, v, is zero($i_i > 0$, v_i=0), and a *reverse biased region* where the independent variable is v and the dependent variable, i, is zero($v_i < 0$, i_i=0). It is switched 'ON' by a *forward current* and switched 'OFF' by a *reverse voltage*.Semiconductor diodes (junction diodes) are available in ICs. We will discuss diodes after we present active devices because active devices are realised using p-n junctions. Diodes are useful as switches. Ideal switches dissipate no power and are very attractive for signal processing.

3 Two Port Networks

3.1 Two Port Parameters

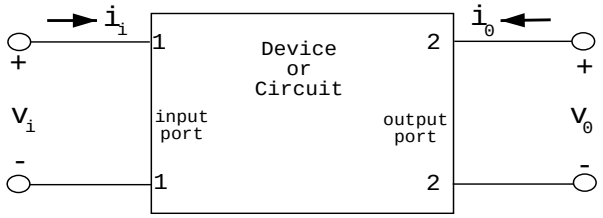

Figure 2: Two-Port Signal Processing Element

Figure 2 shows a block diagram of a two-port or four-terminal signal processing element. If one terminal is common to the input and output, this reduces to a three-terminal two-port. Such a system has four variables and any two can be chosen as independent variables. The other two will then be dependent on the two independent variables. Depending on the choice of dependent variables, we can envision four different types of parameters, and the various linear two-port networks can be described as shown in equations 6 - 13 (It is assumed here that each port has one dependent variable, and one independent variable)

$$v_i = Z_i \cdot i_i + Z_r \cdot i_0 \tag{6}$$
$$v_0 = Z_f \cdot i_i + Z_0 \cdot i_0 \tag{7}$$

Open-Circuit or Z-parameters

$$i_i = Y_i \cdot v_i + Y_r \cdot v_0 \tag{8}$$
$$i_0 = Y_f \cdot v_i + Y_0 \cdot v_0 \tag{9}$$

Short-Circuit or Y-parameters: Dual of Z-parameters

$$v_i = h_i \cdot i_i + h_r \cdot v_0 \tag{10}$$
$$i_0 = h_f \cdot i_i + h_0 \cdot v_0 \tag{11}$$

h-parameters

$$i_i = g_i \cdot v_i + g_r \cdot i_0 \tag{12}$$
$$v_0 = g_f \cdot v_i + g_0 \cdot i_0 \tag{13}$$

g-parameters

3.2 The Ideal Amplifier: The Nullator-Norator Concept

We can now use these parameter definitions to describe the ideal amplifier. Before we do that, let us also describe independent voltage and current

sources. Figure 3 shows a voltage source along with its load. The voltage source is ideal if R_s is zero. In reality, though, the series impedance does not go to zero, and the voltage source is rendered close to ideal by making the load impedance, R_L, much larger than R_s. Figure 4 shows a current source along with its load. In this case, the source is ideal if R_s is infinity. In practice, though, one can obtain a close-to-ideal behaviour by making the load impedance, R_L, much smaller than R_s. The ideal load for a practical voltage source is an open-circuit ($R_L = \infty$) while the ideal load for a practical current source is a short-circuit ($R_L = 0$)

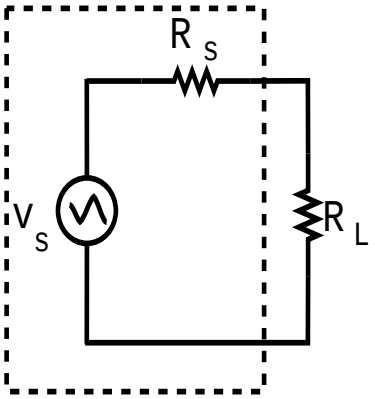

Figure 3: Voltage Source: Thevenin Equivalent

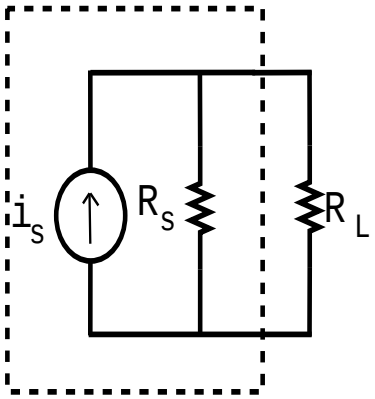

Figure 4: Current Source: Norton Equivalent

Ideal amplifiers can be viewed as controlled sources at the output port with the input acting as the ideal load for the corresponding source.

For instance, an ideal voltage-controlled voltage source (VCVS) can be represented by the 'g' matrix shown in equation 14. The forward transfer parameter is equal to the voltage gain. All the other terms in the matrix are zero.

$$g = \begin{bmatrix} 0 & 0 \\ g_f & 0 \end{bmatrix} \tag{14}$$

By using the same method, we can also represent the ideal current-controlled current source (CCCS) by the 'h' matrix as shown in equation 15. The forward transfer parameter is equal to the current gain. All the other terms in the matrix are zero.

$$h = \begin{bmatrix} 0 & 0 \\ h_f & 0 \end{bmatrix} \tag{15}$$

We further have $[Y]$ and $[Z]$ matrices representing the ideal voltage-controlled current source (VCCS) and current-controlled voltage source (CCVS), respectively. In all cases, the forward transfer parameter is finite while all the other parameters are zero.

The four ideal controlled-sources lead to the following amplifiers: voltage amplifier (VCVS), current amplifier (CCCS), transconductance amplifier (VCCS), and transresistance amplifier (CCVS). It should be noted here that each of these ideal controlled-sources can only be uniquely represented by one type of parameter (Why?).

An important point to note at this juncture is that our aim is to realize one of these amplifiers with the forward transfer parameter made independent of time, temperature, and supply voltage variations. In some cases, it might also be required that the gain be independent of frequency (wide-band) and voltage or current-level (large dynamic range - linear).

VCCS and CCVS amplifiers are more basic than the other two controlled sources. Once we obtain these two, we can cascade them to obtain the other two.In order to therefore characterize amplifier design in a unified manner, we will define what is called the immittance matrix (immaterial of what parameter we choose) as described in equation 16. p_i and p_0 are input and output self-immittances, while p_r and p_f are reverse and forward transfer immittances. An ideal amplifier will have $\mathrm{p}_i = \mathrm{p}_0 = \mathrm{p}_r = 0$.

$$p = \begin{bmatrix} p_i & p_r \\ p_f & p_0 \end{bmatrix} \tag{16}$$

$$p_i = 0, \text{ either it is VC or CC}$$

$$p_0 = 0, \text{ either it is a VS or CS}$$

$$p_r = 0, \text{ it has no feedback}$$

$$p_f = finite, \text{ unilateral transmission in the forward direction}$$

Now, if p_f is made infinity, the amplifier becomes an *operational amplifier* (Op. Amp.). For an Op. Amp, if the output is finite, the input parameter goes to zero (since $p_f = \infty$). In addition, the input self-immittance (p_i) is zero. As a result, both voltage and current go to zero at the input. Such a structure is called a nullator. Since p_f goes to infinity, the output should be capable of sustaining any voltage or current, and the resulting structure is called a norator. The nullator-norator *equivalent circuit* for an Ideal Operational Amplifier is shown in Figure 5. Since we have derived it based on the immittance matrix, we can conclude that the ideal operational amplifier can be designed starting from any of the four types of amplifiers.

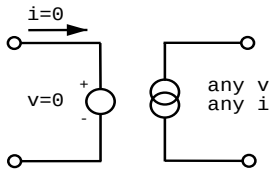

Figure 5: Nullator-Norator Equivalent Circuit of a Differential Input Differential Output Op-Amp(DIDO)

Figures 6 and 7 show equivalent circuits for Differential-Input Single-Ended Output and Single-Ended Input Single-Ended Output Op-Amps, respectively while figures 8, 9 and 10 show nullor equivalents of well known building blocks.

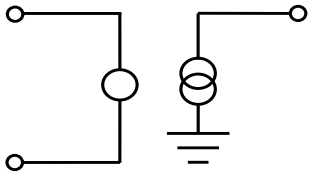

Figure 6: Nullator-Norator Equivalent Circuit of a Differential Input Single-Ended Output Op-Amp (DISO)

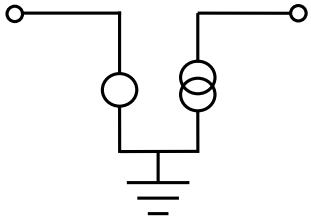

Figure 7: Nullator-Norator Equivalent Circuit of a Single-Ended Input Single-Ended Output Op-Amp (SISO)

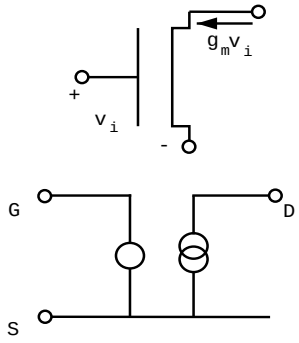

Figure 8: Nullator-Norator Equivalent Circuit of a MOS transistor

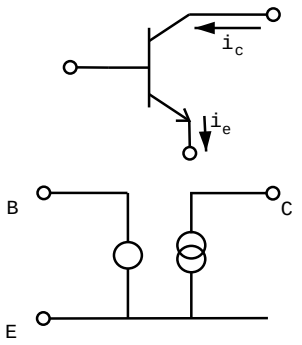

Figure 9: Nullator-Norator Equivalent Circuit of a BJT

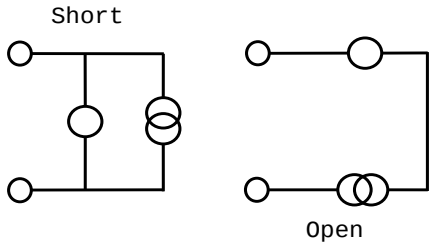

Figure 10: Nullator-Norator Equivalents for Open and Short Circuits

3.3 Differential-Input Differential-Output (DIDO) for a Two-port Network

Before we discuss the realization of the various controlled-sources in single-ended and differential form, let us discuss some of the important features, and benefits, of a differential-input, differential-output two-port network. Figure 11 shows the various currents and voltages involved in a differential network.

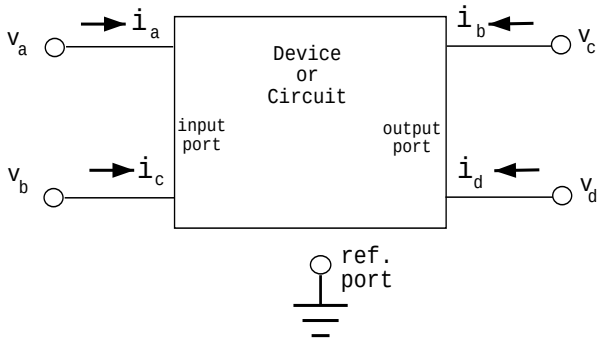

Figure 11: A Differential-Input Differential-Output Two-port Network

Referring to figure 11, v_a and v_b form the input terminal voltages while v_c and v_d form the output terminal voltages. All voltages are measured with reference to a common port as shown in the figure. Such a structure can be considered as a differential-input, differential-output network if the network between the input and output terminals is symmetric. Symmetric networks can be easily fabricated in IC design. We will presently see how such symmetric networks give us signal processing advantages.

We can split v_a and v_b as follows.

$$v_a = \frac{v_a + v_b}{2} + \frac{v_a - v_b}{2} \tag{17}$$

$$v_b = \frac{v_a + v_b}{2} - \frac{v_a - v_b}{2} \tag{18}$$

By expressing it in the above manner, we can obtain a common signal part ($v_{ic} = \frac{v_a+v_b}{2}$) and a differential signal part ($v_{id} = v_a$ - v_b).

We will now consider an example where the advantages of this technique - visualization of the excitation of a symmetric network with asymmetric signals - are demonstrated.

Consider the circuit shown in figure 12. Voltages v_a and v_b are given to be 6sinωt and 4sinωt, respectively. We need to compute the voltages v_{01} and v_{02}.

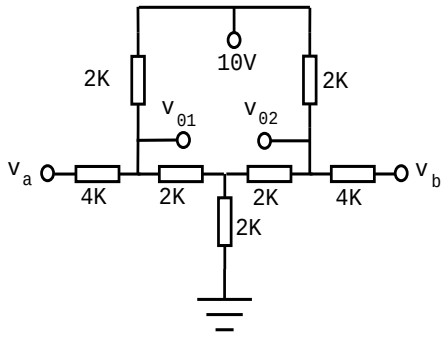

Figure 12: Example Circuit

Let us begin by computing the common-mode and differential-mode voltages.

$$v_{id} = 6sin\omega t - 4sin\omega t = 2sin\omega t \tag{19}$$

$$v_{ic} = \frac{6+4}{2} sin\omega t = 5sin\omega t \tag{20}$$

We will first compute the response to the common-mode voltage. To do that, let us redraw the circuit as shown in figure 13

It is easy to see now that section AB will carry no current. We can hence decouple the two sub-networks as shown in figure 14

By using superposition of sources, we can easily show that $v_{01} = v_{02} = 5 + 1.25\sin\omega t$.

To summarize what we have done, the resistance of 1K at the common point is represented as two equal resistors of 2K each in shunt. Since there is no current flow in the wire connecting the two resistors, it can be split and the circuit itself breaks up as two identical circuits and we need to analyze only one of the circuits to obtain the answer as $v_{01} = v_{02}$ for all common-mode excitations.

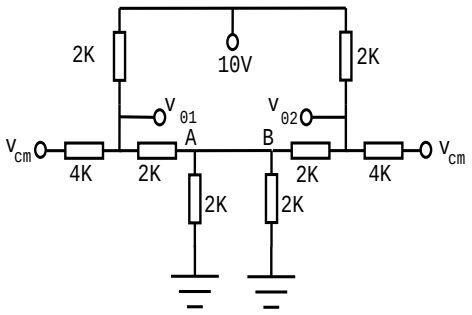

Figure 13: Response to the Common-Mode Input

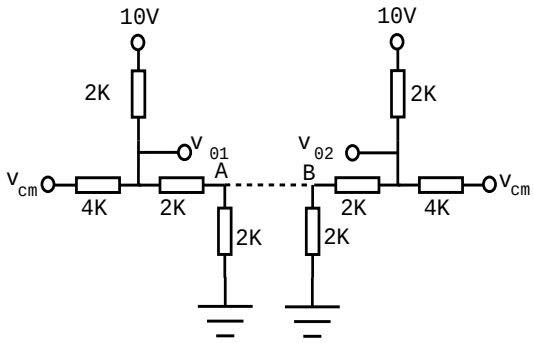

Figure 14: Simplified Circuit Diagram for Common-Mode Input

We will now compute the response of the system to the differential-voltage.Since the input is now differential, all the points of symmetry in the circuit will see no ac swing at all. Hence, they can be considered as 'ac ground'. The circuit to be solved now becomes much simpler and is shown in figure 15.

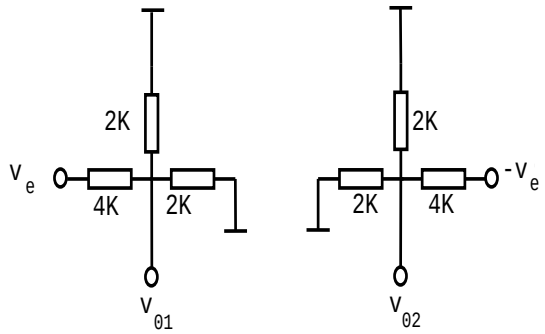

Figure 15: Simplified Circuit Diagram for Differential-Mode Input

$$v_e = \frac{v_{id}}{2} = 1sin\omega t \tag{21}$$

$$v_{01} = -v_{02} = \frac{1}{5} \times 1sin\omega t = \frac{1}{5}sin\omega t \tag{22}$$

$$v_{01} - v_{02} = \frac{2}{5}sin\omega t \tag{23}$$

It must be noted here that the output (v_{01} - v_{02}) is *independent* of the input common-mode signal as well as the supply voltage. Such a circuit can hence be used to reject common-mode. Therefore, if the signal appears as differential-mode at the input, and if the noise appears as a common-mode signal at the input or at the supply or in both places, it is rejected at the differential output. This can result in improvement in signal-to-noise ratio. This is why differential realizations are very popular in most IC designs today. To rephrase, the equivalent for the network for common-mode can be made to look different from that of the differential-mode in a symmetric structure. It is this advantage that is exploited in IC design for improving S/N ratio.

We will now consider another example wherein differential operation at the input becomes necessary. Instrumentation amplifiers are normally needed

in making brdige-type measurements of resistance variation caused either by temperature variation (as in thermistors) or in strain gauges due to stress (as in pressure sensors and velocity sensors). It is well known that strain gauges are resistors whose resistance increases due to expansion and decreases due to compression. These are arranged in a cantilever beam such that the top surface undergoes a change of R + ΔR when the bottom surface undergoes a change of R - ΔR. The equivalent circuit of such a strain gauge bridge is shown in figure 16.

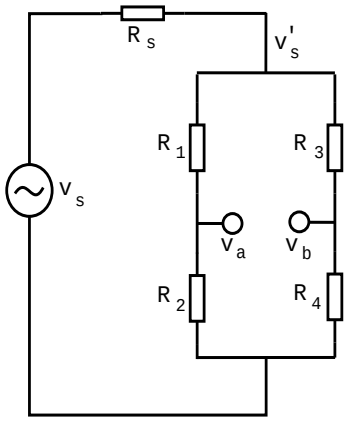

Figure 16: Strain-Gauge Bridge

$$\text{Let } R_1 = R_4 = R + \Delta R; R_2 = R_3 = R - \Delta R \tag{24}$$

$$v_a - v_b = \frac{R - \Delta R}{2R} v_s - \frac{R + \Delta R}{2R} v_s^{'} \tag{25}$$

$$v_a - v_b = -\frac{\Delta R}{R} v_s^{'} \tag{26}$$

$$\tag{27}$$

Common-mode Output Voltage, v_{ic}, is given by,

$$v_{ic} = \frac{v_a + v_b}{2} \tag{28}$$

$$v_{ic} = \frac{1}{2} \cdot \frac{R - \Delta R + R + \Delta R}{2R} \cdot v_s^{'} \tag{29}$$

$$v_{ic} = \frac{v_s^{'}}{2} \tag{30}$$

The output differential voltage is linear with respect to ΔR and has double the sensitivity of a bridge with single transducer. Under a balanced condition, ΔR = 0 and v_a - v_b = 0.

It is now required to design a differential-input amplifier such that it can reject the common-mode voltage of $\frac{v_s^{'}}{2}$ and amplify the differential-mode signal of $-\frac{\Delta R}{R} \cdot v_s^{'}$.

Let us define

$$v_0 = v_{id} \cdot A_d + v_{ic} \cdot A_c \tag{31}$$

where A_d is known as the differential-mode gain of the amplifier and A_c is termed as the common-mode gain.

$$v_0 = v_{id} \cdot A_d \left(1 + \underbrace{\frac{v_{ic}A_c}{v_{id}A_d}}_{error} \right) \tag{32}$$

In such systems, if it is required that a 1% error be maintained for 1% variation in R.

$$\frac{v_{ic}}{v_{id}} = \frac{\frac{v_s^{'}}{2}}{\frac{\Delta R}{R} v_s^{'}} = \frac{R}{2\Delta R} = 50 \tag{33}$$

$$error = \frac{v_{ic}A_c}{v_{id}A_d} = 50 \times \frac{A_c}{A_d} = \frac{1}{100} \tag{34}$$

$$CMRR = \frac{A_c}{A_d} = \frac{1}{5000} \tag{35}$$

The ratio of the common-mode gain to the differential-mode gain is called the Common-Mode Rejection Ratio (CMRR). The CMRR of an ideal differential amplifier is ∞

3.4 Realisation of Controlled Sources Using the Nullator-Norator Concept

We have now understood the basic equivalent circuits of the Op-Amp (DIDO, DISO and SISO), BJT, MOSFET, Open and Short Circuits as well as the features and benefits of a differential-input differential-output network. Now we can synthesize some of the most important building blocks using these equivalents in both single-ended and differential form. Figures 17 and 18 show different realizations of a VCVS with a gain of unity, and a CCCS with a gain of unity, respectively.

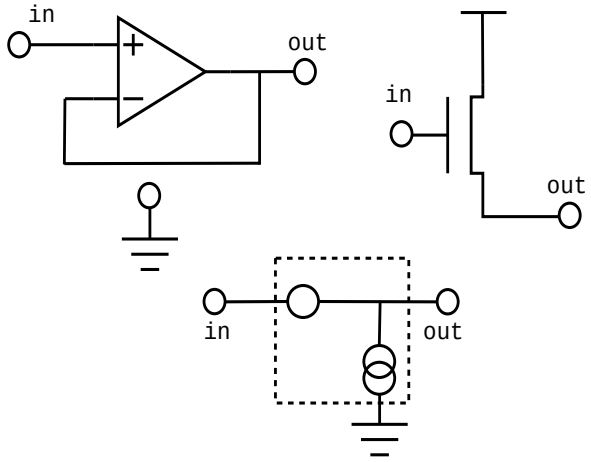

Figure 17: Representations of a VCVS with Unity Gain

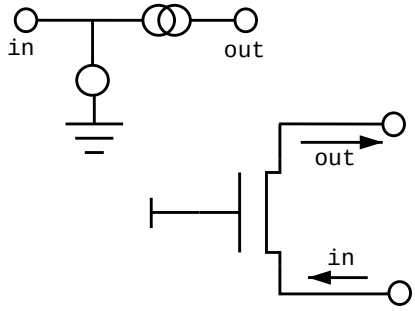

Figure 18: Representations of a CCCS with Unity Gain

We will now consider the realization of a transconductance amplifier using a conductance, nullators and norators. Transconductance amplifiers are voltage-controlled current sources (VCCS). The nullator must come *in series with the input voltage* to make it voltage-controlled and the norator must come in series with the conductance to sustain the current G·V. Figure 19 shows two realisations of a transconductance amplifier.

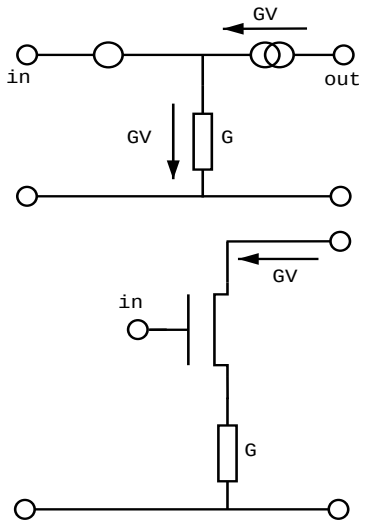

Figure 19: Realizations of a VCCS

The transconductance amplifier can also be realised as a differential-input differential-output circuit. Figure 20 shows several examples of such realizations. It maybe worth noting that transistor versions (BJT or MOS) need a junction to be formed between the nullator and the norator. The DIDO Op-Amp version of the circuit does not have any such restrictions. DISO Op-Amp implementations need the norators to be grounded.

The other building block is the Current-Controlled Voltage Source (CCVS) or the Transresistance Amplifier. We will now explore realzations of this building block. The nullator must come in shunt with the input to make it current-controlled and to maintain $v_i = 0$, and the norator must be in shunt so that it can accept any input current, I_i, and also source any current that is required by the load. The controlling element (the resistor) will appear between the norator and the nullator and converts the input current to voltage. Figure 21 shows examples of single-ended realizations of this amplifier while

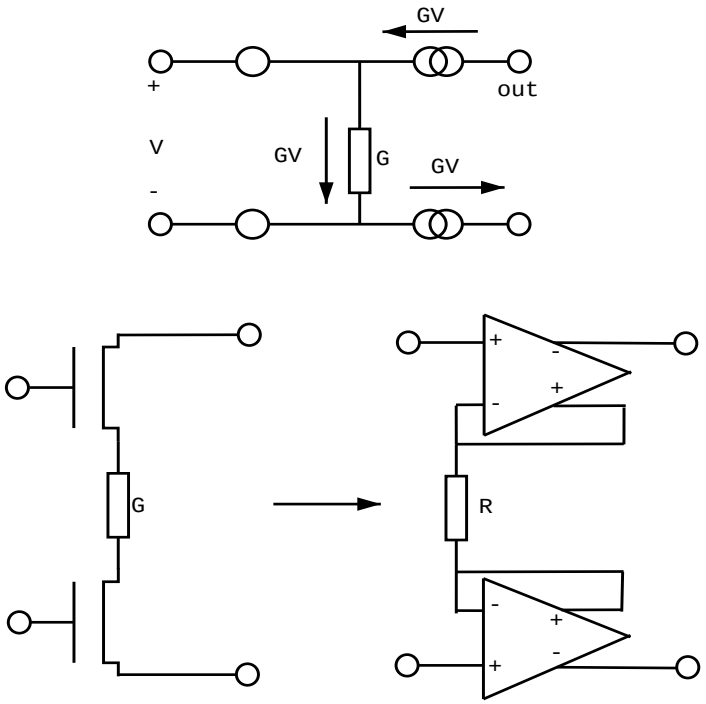

Figure 20: Realizations of a Differential-Input Differential-Output VCCS

figure 22 shows differential realizations. In order to realize the transistor-based differential equivalent of the CCVS, we will need to understand the concepts of ac ground and balanced circuits. We will hence explore transistor-based realizations of the differential-input differential-output CCVS when we discuss the design of practical differential amplifiers.

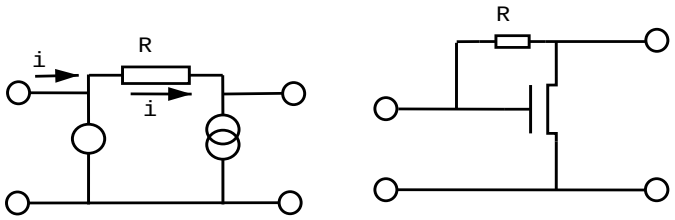

Figure 21: Realizations of Current-Controlled Voltage Sources (CCVS)

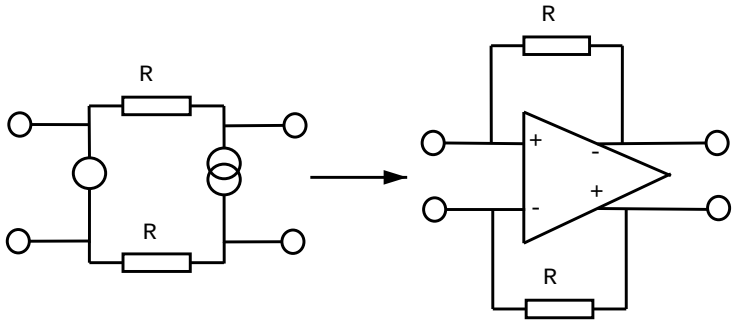

Figure 22: Realizations of Differential-Input Differential-Output Current-Controlled Voltage Sources (CCVS)

We can now realize VCVS and CCCS by cascading VCCS and CCVS or CCVS and VCCS, respectively. Figure 23 shows single-ended realizations of the VCVS amplifier while figure 24 shows single-ended realizations of the CCCS amplifier. Figure 25 shows differential realizations for the two circuits.

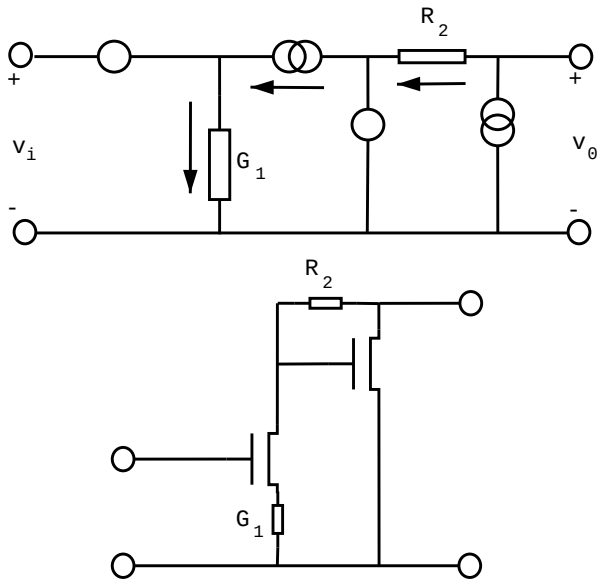

Figure 23: Realizations of VCVS as a Cascade of VCCS and CCVS: $v_0 = G_1 \cdot R_2 \cdot v_i$

4 Simulation of Negative Resistances and Inductors

4.1 Negative Resistance Simulation

A lot of applications require the use of loss-free loads (e.g. Oscillators). Ideally-lossless passive elements, due to the properties of the materials from which they are fabricated, and due to the fabrication process, have associated parasitics, and are not loss-free. To compensate for these losses, a *negative resistance* element is required. Unlike positive resistances which dissipate power, these elements deliver power. Hence, these are active elements.

Figure 26 shows the current and voltage polarities for positive and negative resistances. To achieve a negative resistance, we need to reverse the direction of current for a given voltage or reverse the polarity of the voltage for a given current. A nullator-norator based method to realize this reversal of the direction of current is shown in figure 27.

Based on the nullator-norator realization shown in figure 27, two possible

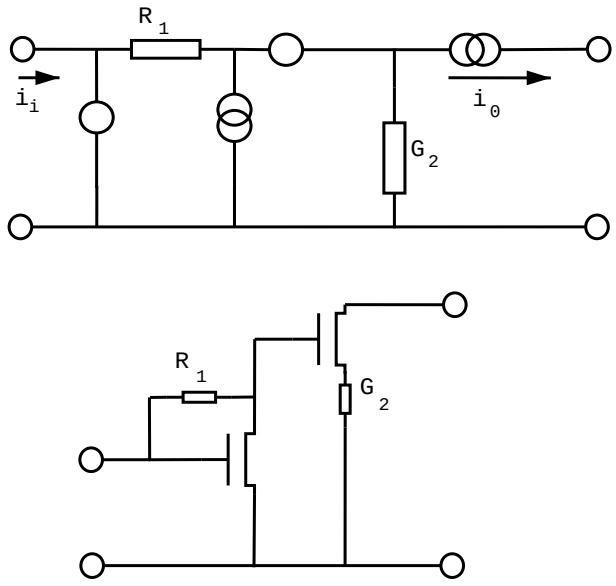

Figure 24: Realizations of CCCS as a Cascade of CCVS and VCCS: $i_0 = G_2 \cdot R_1 \cdot i_i$

transistor realizations exist. Using the nodes labelled in the figure, they are a) Gate-M1:2; Drain-M1:3; Source-M1:1, Gate-M2:3; Drain-M2:2; Source-M2:4 and b) Gate-M1:1; Drain-M1:4; Source-M2:2, Gate-M2:4; Drain-M2:1; Source-M2:3 (We derived the norator-nullator equivalent of a MOS transistor in the previous section - figure 8). Figure 28 shows the two MOS-based realizations. The Op-Amp based circuit can also be realized from the nullator-norator equivalent. A differential-input differential-output realization is shown in Figure 29.

4.2 The Negative Impedance Converter/Negative Impedance Inverter (NIC/NII)

The reversal of the direction of current can also be achieved by using one nullator-norator pair, and three resistances. The circuit is shown in figure 30. In general, one can use such a circuit as a negative impedance inverter/converter(NII/NIC) by replacing the resistors in figure 30 by other (and if necessary, a combination of) passives. The circuit is shown in fig-

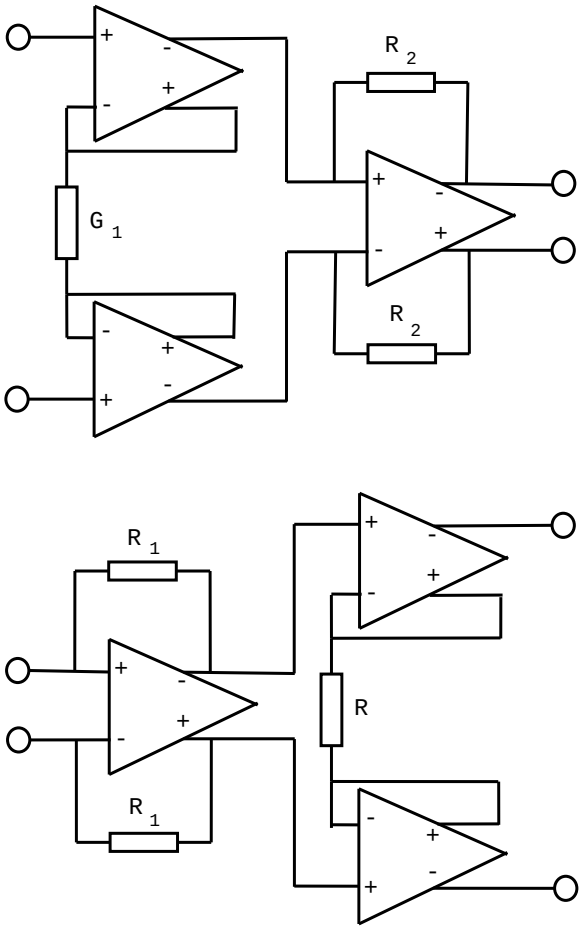

Figure 25: Differential-Input Differential-Output Realizations of VCVS and CCCS as a Cascade of VCCS and CCVS, and CCVS and VCCS, respectively

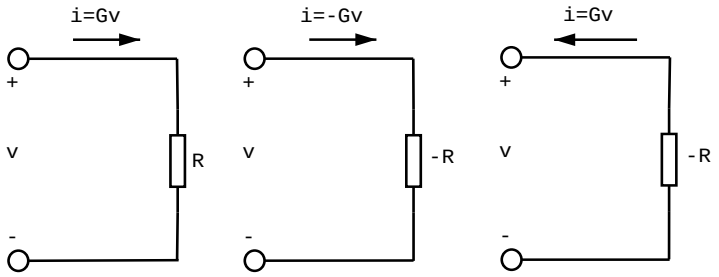

Figure 26: Negative Resistance: Current Direction and Voltage Polarity

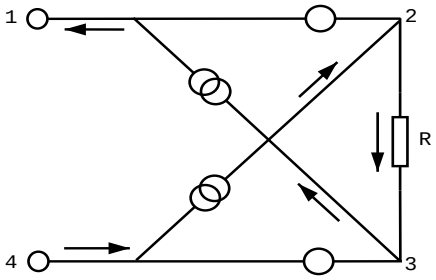

Figure 27: Nullator-Norator based Realizations of a Negative Resistance. The arrows indicate the direction of current flow.

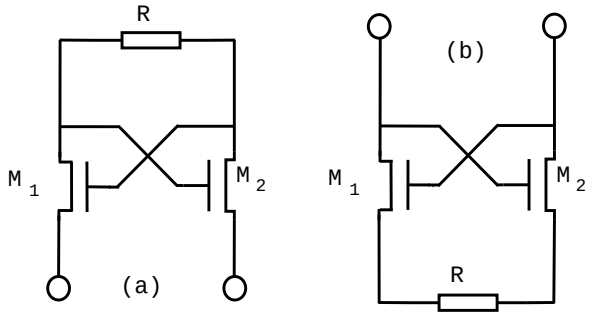

Figure 28: MOS-based Realizations of Negative Resistance

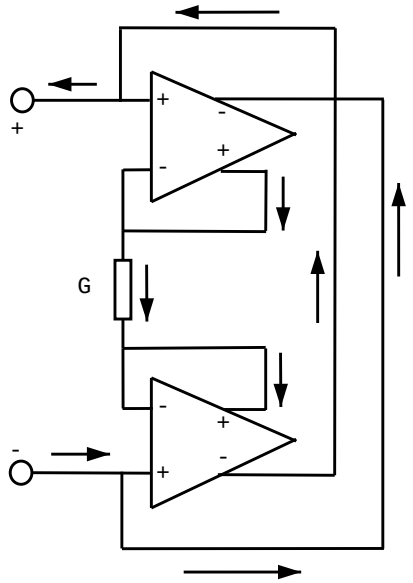

Figure 29: Differential-Input Differential-Output Op-Amp based Realization of a Negative Resistance. The arrows indicate the direction of current flow.

ure 31 while the relation between the component that is realized and the passives used in the realization is described in equation 36. One example of a circuit realization (using differential-input single-ended output Op-Amps) is shown in figure 32. We will explore this circuit in more detail in the following section.

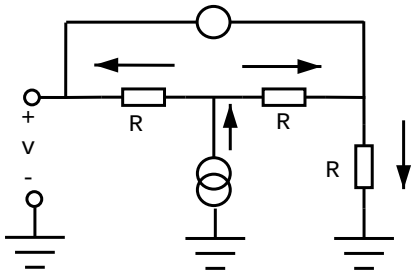

Figure 30: Realization of a Negative-Resistance Element using 1 Nullator-Norator Pair. The arrows indicate the direction of current flow.

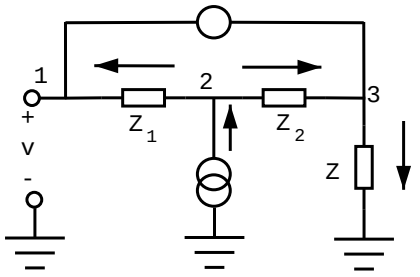

Figure 31: The Negative Impedance Converter/Negative Impedance Inverter (NII/NIC) Circuit. The arrows indicate the direction of current flow.

$$
\begin{aligned}
v_3 = v_1 = v_{in} \\
i_Z = \frac{v_{in}}{Z} \\
i_{Z_2} = i_Z = \frac{v_{in}}{Z} \\
v_2 = v_{in} \cdot (1 + frac Z_2 Z) \\
i_{Z_1} = \frac{v_2 - v_{in}}{Z_1} = v_{in} \cdot \frac{Z_2}{Z \cdot Z_1} \\
Z_{in} = \frac{-v_{in}}{i_{Z_1}} = \frac{-Z \cdot Z_1}{Z_2}
\end{aligned} \tag{36}
$$

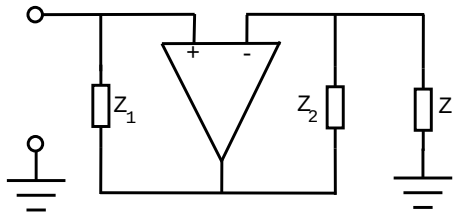

Figure 32: Op-Amp Realization of the NII/NIC Circuit

4.3 Inductance Realization using the NII/NIC

In the previous section, we derived the driving-point impedance of the NII/NIC circuit. We will use that equation (shown below) as a starting point for our discussion on simulating inductances.

$$Z_i = \frac{-Z \cdot Z_1}{Z_2}$$

In the above equation, if $Z = Z_1 = R$, the circuit acts as a NII. If $Z_1 = Z_2 = R$, it acts as a NIC. In the former case, for example, if we choose Z_2 to be a capacitance, and choosing Z_1 and Z to be resistances, we will obtain a negative inductance. To convert this into a positive inductance, or in other words, to convert the circuit to a positive impedance inverter/converter (PII/PIC), we can cascade it with another NII/NIC as shown in figure 33.

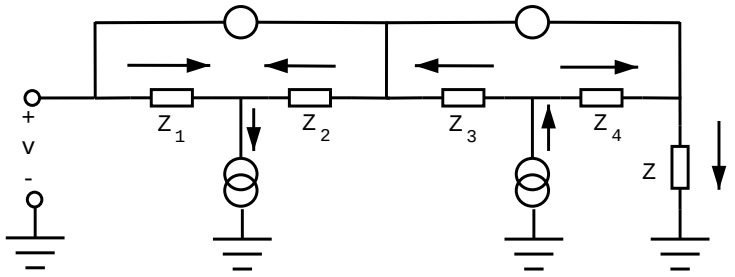

Figure 33: The Positive Impedance Converter/Inverter. The arrows indicate the direction of current flow.

$$Z_{in} = \frac{Z_3 \cdot Z_1 \cdot Z}{Z_2 \cdot Z_4} \tag{37}$$

The relation between the driving-point impedance, Z_{in}, and the various impedances in the circuit is given in equation 37. Let us now consider some special cases of this circuit. We will assume that Z_1, Z_3 and Z are resistances. Let us further assume that Z_2 is also a resistance. In such a scenario, this circuit will invert the nature of Z_4. In other words, in such a scenario, the circuit will convert a capacitance to an inductance, an inductance to a capacitance, an open-circuit to a short-circuit and a short-circuit to an open-circuit. Such a circuit is called a *Gyrator*. We should note that we could have just as well chosen Z_4 as a resistance, and inverted the nature of Z_2.

In an IC, this idea can be used to convert all LC circuits to active-RC circuits by replacing the inductance with a *simulated* inductance. This is particularly convenient since inductors are not compatible with most IC technologies.

At this juncture, we can demonstrate the power-of-synthesis of the basic concept of nullators and norators in coming up with practically different circuit topologies which perform ideally the same network function. Starting with the PIC/PII, we can generate two gyrator circuits: one with Z_4 as a capacitance, and the other with Z_2 as a capacitance. All the other elements are resistors. Each of the above topologies result in two Op-Amp equivalents (obtained by pairing nullators and norators suitably).

Further, since the two nullators share a port, there can be no voltage or current flow between the ports that they do not share. We can, hence, put a third nullator between those two ports, and remove one of the other

two nullators. Each such technique will result in four gyrators. Since three nullator combinations are possible, we can envision twelve gyrator realizations starting from the first gyrator circuit. These circuits can be simulated in the presence of non-idealities, and the best topology for that particular process/application can be chosen. We will explore this is more detail when we discuss the design of practical Op-Amps.

Before we conclude this chapter, we will discuss an application of gyrators in the design of filters. Consider the RLC circuit shown in figure 34. The transfer function of such a circuit is derived in equation 38.

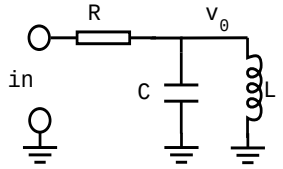

Figure 34: RLC Tank Circuit

$$\begin{aligned}
\frac{v_0}{v_i} &= \frac{\frac{1}{R}}{\frac{1}{R} + sC + \frac{1}{sL}} \\
\frac{v_0}{v_i} &= \frac{\frac{sL}{R}}{s^2LC + \frac{sL}{R} + 1} \\
\frac{v_0}{v_i} &= \frac{\frac{s}{\omega_0 Q}}{\frac{s^2}{{\omega_0}^2} + \frac{s}{\omega_0 Q} + 1}
\end{aligned} \tag{38}$$

Such a circuit is called a RLC tank circuit. It can act as a band-pass filter with centre frequency, ω_0, given by $\omega_0 = \frac{1}{\sqrt{LC}}$ and the quality factor, Q, given by $Q = \frac{R}{\omega_0 L} = \omega_0 RC = R\sqrt{\frac{C}{L}} = \frac{\omega_0}{BW \text{ in rad/s}}$.

We can now simulate the inductor using gyrators such that $L = C{R_1}^2$. In this particular case, we will obtain $\omega_0 = \frac{1}{RC}, Q = \frac{R}{R_1}$. The final circuit is shown in figure 35. The reader is recommended to prove that the circuit indeed simulates an inductance. (*Hint*: Derive the driving-point impedance by calculating the current assuming that the gyrator is driven by a voltage source)

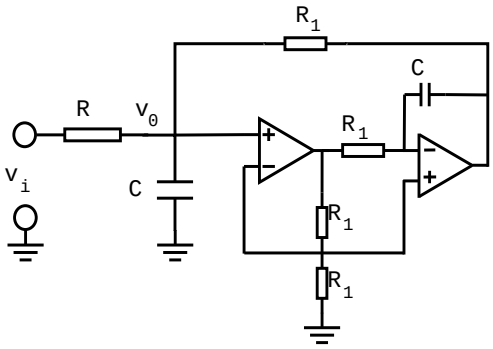

Figure 35: Inductor-free Tank Circuit - The Inductor is Simulated using an Active-RC Circuit

5 Exercises

[1]. For the two-port networks shown in figures 36 to 39, determine the appropriate two-port parameters.

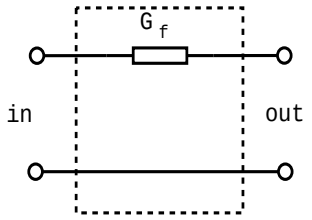

Figure 36: Evaluate Y-parameters

Note that for passive networks $Y_f = Y_r$; $Z_f = Z_r$; h_f = -h_r and g_f = -g_r.

[2]. (a) For a two-port network, express the Z-parameters in terms of its Y-parameters.

(b) For a two-port network, express the g-parameters in terms of its h-parameters.

(c) Show that the input-port immittance parameter, p_{in}, for a given load immittance, p_L, can be expressed as $p_{in} = p_i - \frac{p_r \cdot p_f}{p_0 + p_L}$

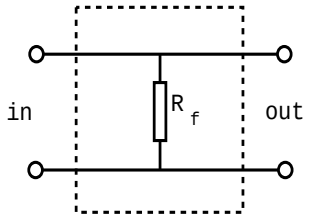

Figure 37: Evaluate Z-parameters

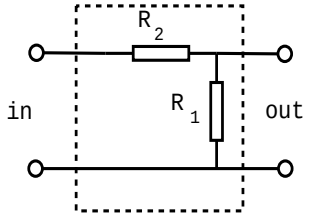

Figure 38: Evaluate g-parameters

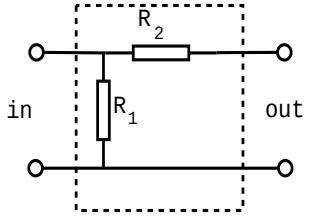

Figure 39: Evaluate h-parameters

(d) Show that the output port immittance parameter, p_{out}, for a given source immittance, p_S, can be expressed as $p_{out} = p_0 - \frac{p_r \cdot p_f}{p_i + p_S}$

(e) Show that the forward gain of a two-port network is given by $\frac{-p_f}{p_0 + p_L}$ and reverse gain is given by $\frac{-p_r}{p_i + p_S}$ and hence the loop gain, g_l, is defined as $\frac{p_f \cdot p_r}{(p_0 + p_L) \cdot (p_i + p_S)}$. The sign of the loop gain determines the nature of the feedback. If the loop gain is positive, it is positive feedback, and if the loop gain is negative, it is negative feedback. We will use this fact when we discuss feedback theory.

[3]. Determine the type of controlled-sources and estimate the appropriate forward transfer parameter for the circuits shown in figures 40 and 41. Realize the transistor and Op-Amp versions of the same.

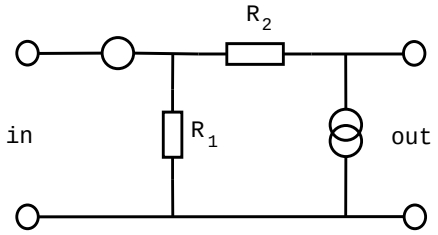

Figure 40: Figure for Problem 3(a)

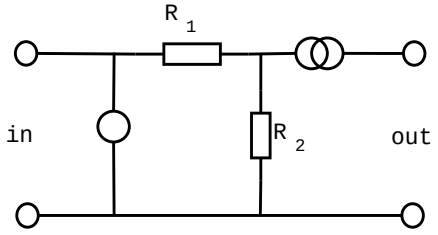

Figure 41: Figure for Problem 3(b)

[4]. Convert the amplifier structure shown in figure 42 into its nullator-norator equivalent and evaluate its voltage gain, current gain, input resistance for a specific load resistance, and output resistance for a specific source resistance.

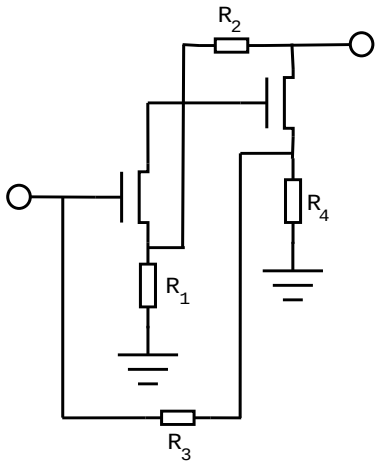

Figure 42: Figure for Problem 4

[5]. (a) The two-port network shown in figure 43 is called a tank circuit. Assume that the capacitor was charged to a voltage of 2 volts at t=0. Sketch v_0 after t=0. This is an LC oscillator. Use L=1nH and C=10pF.

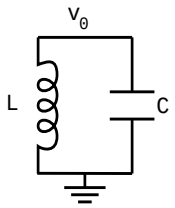

Figure 43: Figure for Problem 5(a)

(b) For the circuit shown in figure 44, sketch v_0 after t=0. Assume that the capacitor was charged to a voltage of 2 volts at t=0. Use L=1nH, C=10pF and R=1K.

(c) Simulate the inductor of 1nH using ideal op-amps, resistors and capacitors. An RC osciallator can thus be realised by replacing the inductance of (a) by this simulated inductance. The loss in (b) can be compensated for by simulating a negative resistance of magnitude R.

[6]. An instrumentation amplifier is to be designed for handling variations

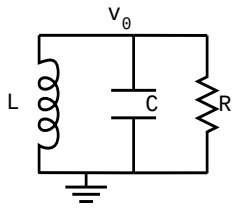

Figure 44: Figure for Problem 5(b)

as low as 1mV over a 1V common-mode signal with an accuracy of 1%. What is the minimum CMRR required in the amplifier?

[7]. For the circuit shown in figure 45, determine v_a, v_b and v_a - v_b. Assume $v_1 = 5 + 4\sin\omega t$ and $v_2 = 5 + 3\sin\omega t$. Use the principles of common-mode and differential-mode excitations for a symmetrical circuit.

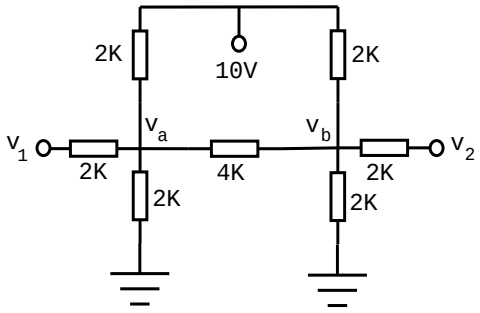

Figure 45: Figure for Problem 7