Back to Basics
Teaching Analog Circuits - an alternate to Superposition

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In a previous article published in UniTI Newsletter Vol-1,Issue1, I discussed how ideas about signal processing using analog ICs can be introduced at networks level – for example, when teaching basic network theorems such as the well known Superposition Theorem. In the article, I introduced two problems, both involving a symmetric network, which is repeated here in Figure 1 for your convenience.

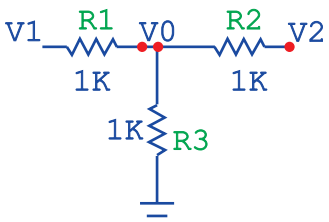


Figure 1 – A simple symmetric circuit

- Problem 1: Find VO when V1 = V2 = +1 V.
- Problem 2: Find VO when V1 = +1V and V2 = -1V.

When I have posed Problem 1 in the class room, the knee-jerk reaction from most students is "zero volts," which, unfortunately, is the incorrect answer. After reading the disappointment in my face, the student would make another attempt and revise the answer to "one volt." I would shake my head in negation, and, after some more audible cranking of the brains, I would elicit the correct answer of "2/3 V" from the student. On the other hand, when I have posed Problem 2 in the classroom, I have often drawn an immediate (and correct) response of "zero volts."

An application of the Superposition Theorem, where the circuit is analyzed with only V1, followed by only V2, followed by a superposition of the results, will, of course, result in the correct result. However, I argue that this is the "network approach" and not the "signal processing approach." In this article, I will dwell on what I consider the right approach for solving problems involving symmetric networks with asymmetric excitation. I recommend splitting the excitation into common and differential mode signals, and apply these signals separately to obtain the composite output.

Here is an important observation:

> At all common output points in a symmetric network, the output due to common mode alone exists. Differential outputs need to be considered only for differential signal input.

Returning to Problem 1, we note that since V1 = V2 = 1V, there is no differential component in the input signal pair. Therefore, we need to only perform common mode analysis. Let us treat the 1K Ohm resistor as a parallel combination of two 2K Ohm resistors, without impacting symmetry. This is illustrated in Figure 2. The circuit now falls apart into two simple series networks, and the output at the common mode can be easily computed as $1/(1+2) \times 2 = 2/3$V, the magic answer that I was looking for! And with far less effort than superposition!

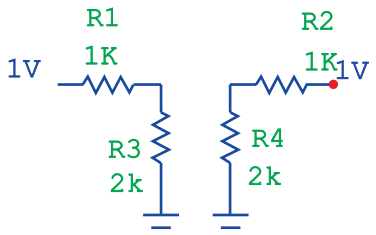


Figure 2 – Common Mode Analysis for Problem 1

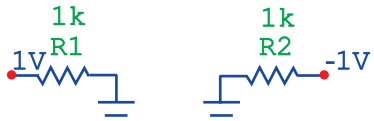
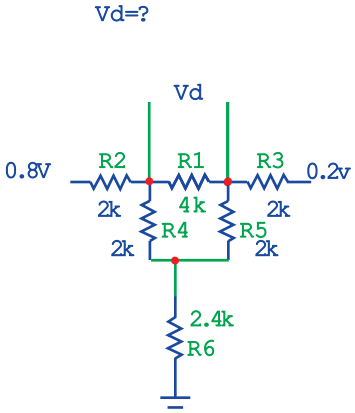


Figure 3 - Differential Mode Analysis for Problem 2

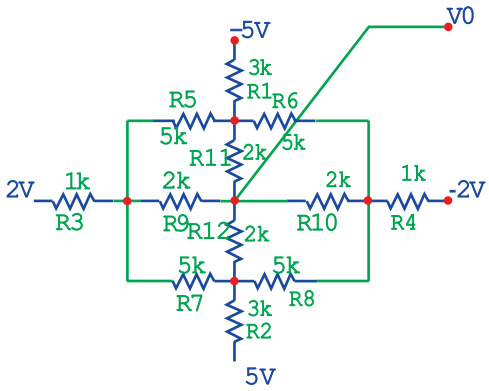
In Problem 2, since V1 = 1V and V2 = -1V, there is no common mode signal. Therefore, we only need to perform a differential mode analysis. Again, using the observation above, the circuit simplifies to what is shown in Figure 3. Again, the differential mode output can be easily seen as "zero volts."

I will leave you with some exercises. Have fun solving them. The answers will be published in the next issue of UniTI newsletter. Feel free to send your answers to me. Readers who send correct answers will be rewarded!

Problem 3. Find Vd in the circuit shown below.

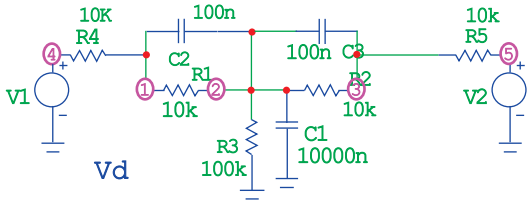


Problem 4. Find V0 in the circuit shown below.

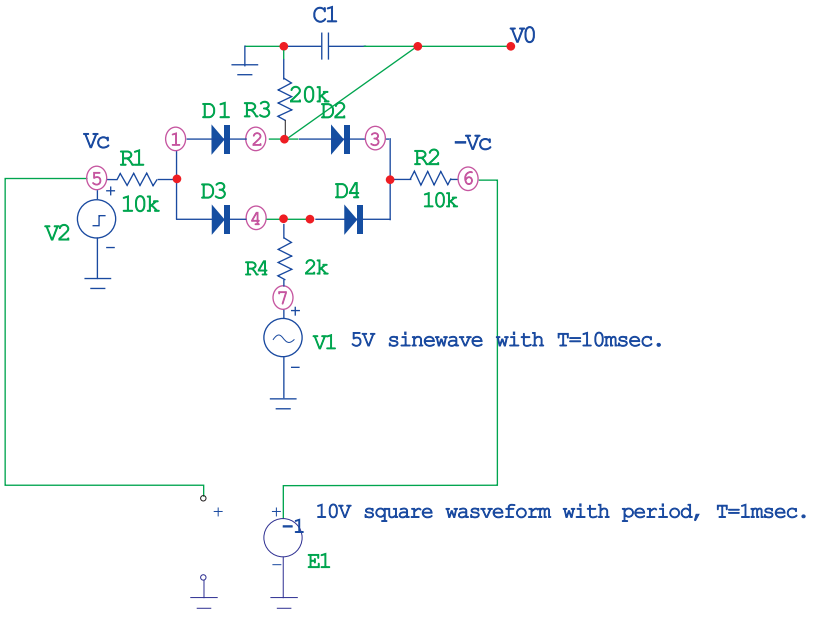


Problem 5.

Determine v(2) & i(R1) in the RC-network shown. V1 is a Square Wave pulse train of 5V amplitude (T=1msec) and V2 is the same train delayed by half period.



Problem 6. Find VO in the circuit shown below.



Problem 7. Find VO in the circuit shown below.